Next Gen Development in Type-C Ecosystem and USB4/TBT4 Update Include LRD Active Cable

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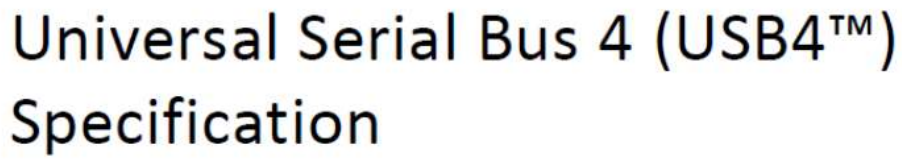
KEYSIGHT TECHNOLOGIES

Agenda

- Technology Overview
- Testing Challenges
- Lessons Learned
- Solutions Summary

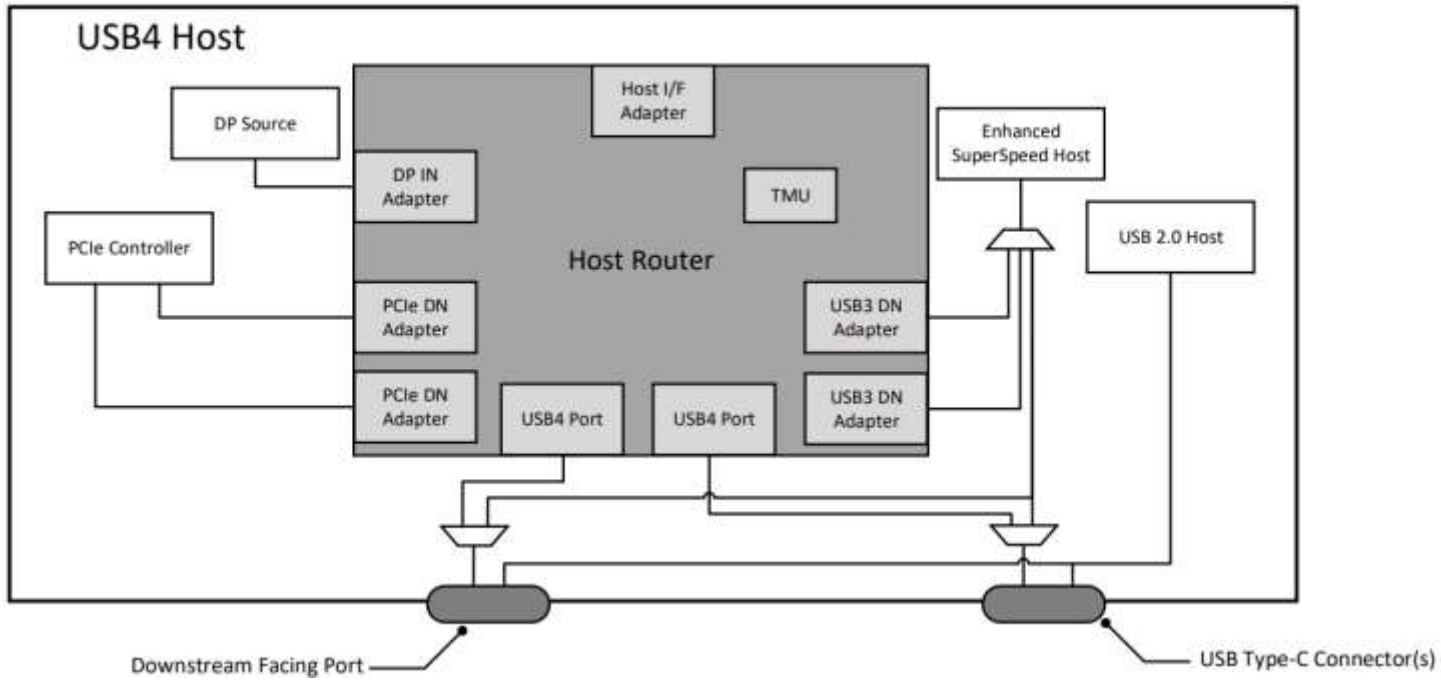
USB4 Technology Overview

- Announced by USB-IF in March 2019
- Spec released September 2019
- Based on the Thunderbolt 3 protocol
- Uses the Type-C connector
- Two 20 Gb/s PHY lanes bonded into one logical 40 Gb/s link
- CTS is available but potential future updates to test methodology
- One Spec and Electrical CTS for USB4/TBT4/TBT3
- Numerous USB4 Products shipping and available on the market
- Driven by 5G adoption



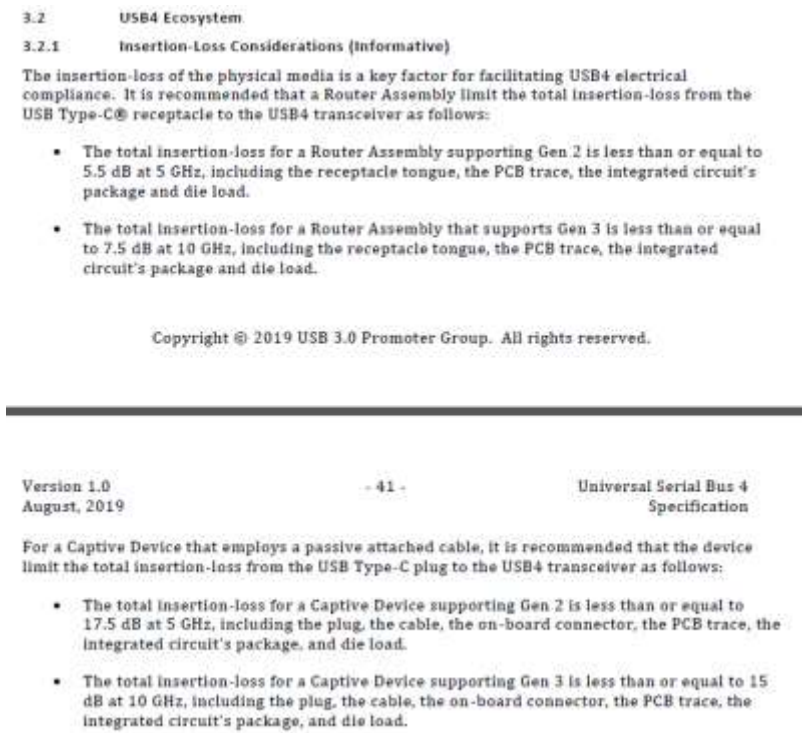
Architecture Overview

- Must test for USB4 with and without retimers
- USB 3.2, USB 2.0, DisplayPort, Thunderbolt compatibility
- **Challenge**: Same port, different standards, similar speeds, different cable losses.



Insertion Loss Budget

- Insertion Loss Budget is the foundation for Silicon or End Products
- USB 3.2 Gen 2 10G has different loss budget
- **Challenge**: Long channel and short/no channel use cases and multiple bit rates and standards over same physical port



3.2 USB4 Ecosystem

3.2.1 Insertion-Loss Considerations (Informative)

The insertion-loss of the physical media is a key factor for facilitating USB4 electrical compliance. It is recommended that a Router Assembly limit the total insertion-loss from the USB Type-C® receptacle to the USB4 transceiver as follows:

- The total insertion-loss for a Router Assembly supporting Gen 2 is less than or equal to 5.5 dB at 5 GHz, including the receptacle tongue, the PCB trace, the integrated circuit's package and die load.
- The total insertion-loss for a Router Assembly that supports Gen 3 is less than or equal to 7.5 dB at 10 GHz, including the receptacle tongue, the PCB trace, the integrated circuit's package and die load.

For a Captive Device that employs a passive attached cable, it is recommended that the device limit the total insertion-loss from the USB Type-C plug to the USB4 transceiver as follows:

- The total insertion-loss for a Captive Device supporting Gen 2 is less than or equal to 17.5 dB at 5 GHz, including the plug, the cable, the on-board connector, the PCB trace, the integrated circuit's package, and die load.
- The total insertion-loss for a Captive Device supporting Gen 3 is less than or equal to 15 dB at 10 GHz, including the plug, the cable, the on-board connector, the PCB trace, the integrated circuit's package, and die load.

Data Rate	Host	Connector	Cable	Connector	Device
5G	10dB	Std A	7.5dB	Std B	2.5dB
5G	10dB	Std A	3.5dB	Micro B	6.5dB
5G	6.5dB	C	7dB	C	6.5dB
5G	10dB	Std A	3.5dB	C	6.5dB
5G	6.5dB	C	4dB	Std B	2.5dB
5G	6.5dB	C	4dB	Micro B	6.5dB
10G	8.5dB	Std A	6dB	Std B	8.5dB
10G	8.5dB	Std A	6dB	Micro B	8.5dB
10G	8.5dB	Std A	6dB	C	8.5dB
10G	8.5dB	C	6dB	Std B	8.5dB
10G	8.5dB	C	6dB	Micro B	8.5dB
10G	8.5dB	C	6dB	C	8.5dB

Speed	Total Budget (dB)	Host (dB)	Cable (dB)	Device (dB)
Gen2 (10G)	23	5.5	12	5.5
Gen3 (20G)	22.5	7.5	7.5	7.5

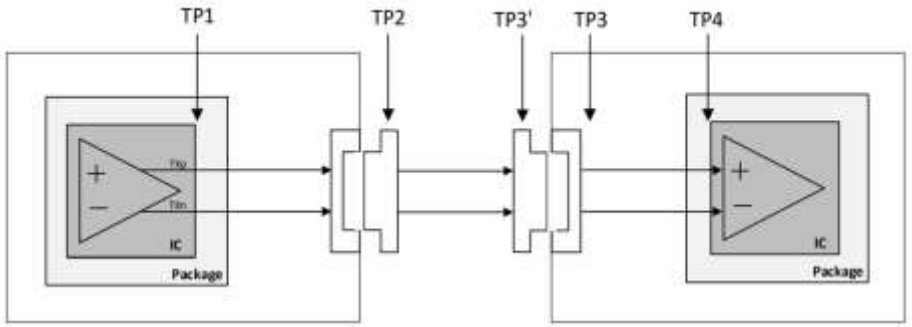
Electrical Compliance Test Points

- TP definition has no set rules
- For USB4, what are the specific test points for TX and RX, short channel and long channel?
- **Challenge**: Imprecise TP understanding invalidates testing

Table 3-2. Electrical Compliance Test Points

Test Point	Description	Comments
TP1	Transmitter IC output	Not used for electrical testing.
TP2	Transmitter port connector output	Measured at the plug side of the connector.
TP3	Receiver port connector output	Measured at the receptacle side of the connector. All the measurements at this point shall be done while applying reference equalization function.
TP3'	Receiver port connector input	Measured at the plug side of the connector.
TP4	Receiver IC input	Not used for electrical testing.

Figure 3-2. Compliance Points Definition



Transmitter Specifications (Short/Long Channel Use Case)

- Traditional voltage, eye, SSC, 10ps min rise/fall times
- Traditional UI, TJ, DDJ jitter decomposition
- **Challenge**: New uncorrelated jitter, phase, retimer measurements, short and long channel use case

Table 3-3. Transmitter Specifications Applied for All Speeds (at TP2)

Symbol	Description	Min	Max	Units	Conditions
RL_DIFF	Differential Return Loss, 0.05-12GHz	--	See Section 3.4.1.2	dB	
RL_COMM	Common Mode Return Loss, 0.05 – 12GHz	--	See Section 3.4.1.3	dB	
TX_EQ	Transmitter Equalization Setting	--	See Section 3.4.1.4		
SSC_DOWN_SPREAD_RANGE	Dynamic range of SSC down-spreading during steady-state	0.4	0.5	%	See Note 3, Note 4, and Figure 3-9.
SSC_DOWN_SPREAD_RATE	SSC down-spreading modulation rate during steady-state	30	33	KHz	See Note 4 and Figure 3-9.
SSC_PHASE_DEVIATION	Phase jitter associated with the SSC modulation during steady-state	2.5	13	ns pp	See Note 1, Note 4, and Figure 3-9.
SSC_SLEW_RATE	SSC frequency slew rate (df/dt) during steady-state	--	1250	ppm/µs	See Note 2, Note 4, and Figure 3-9.
TX_FREQ_VARIATIONS_TRAINING	TX frequency variation during Link training, before obtaining steady-state	--	See Section 3.4.1.1	ppm	See Note 4.
LANE_TO_LANE_SKEW	Skew between dual transmit signals of the same USB4 Port	--	26	ns	See Note 5.
RISE_FALL_TIME	TX rise/fall time measured between 20-80% levels	10	--	ps	Test pattern shall be SQ128 (see Table 8-56).
V_ELEC_IDLE	Peak voltage during transmit electrical idle (one-sided voltage opening of the differential signal)	--	20	mV	See Note 6.
V_TX_DC_AC_COMM	Instantaneous DC+AC voltages at the connector side of the AC coupling capacitors	-0.3 (min1) -0.3 (min2)	1.0	V	See Note 7.

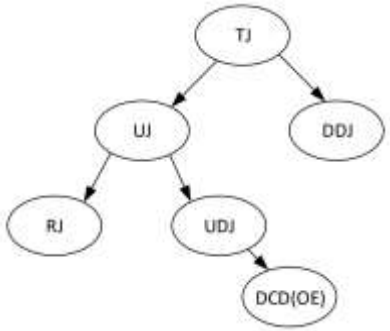


Figure 3-15. TX Mask Notations

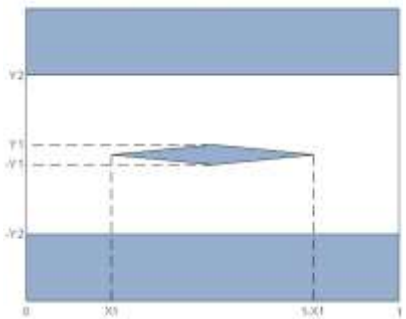
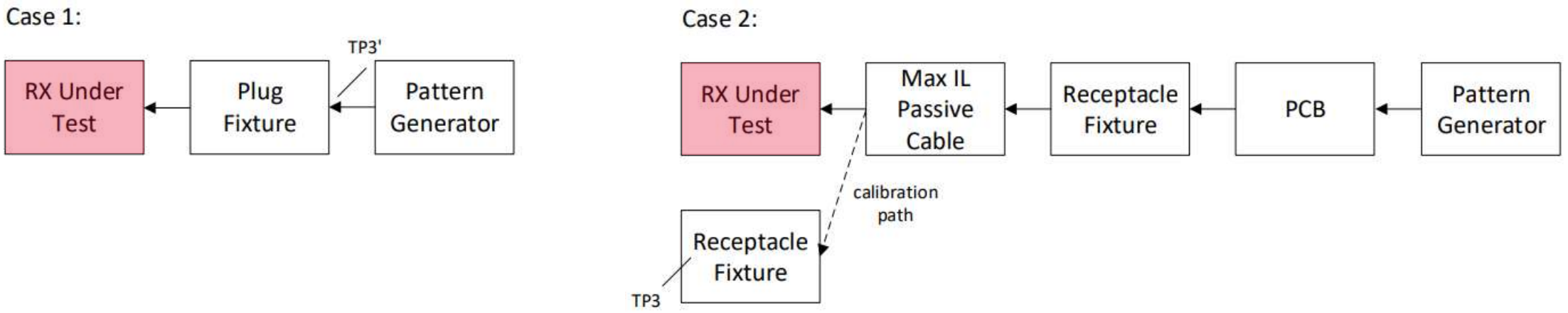


Table 3-6. Gen 2 Transmitter Specifications at TP2

Symbol	Description	Min	Max	Units	Comments
UI	Minimum Unit Interval	99.97	100.03	ps	The minimum UI value corresponds to the Link baseline speed of 10.0 Gbps with an uncertainty range of -300 ppm to 300 ppm. See Note 4.
AC_CM	TX AC Common Mode voltage	--	100	mV pp	
TJ	Total Jitter	--	0.38	UI pp	See Note 2 and Note 3.
UJ	Sum of uncorrelated DJ and RJ components (all jitter components except for DDJ)	--	0.31	UI pp	See Note 2.
DDJ	Data-Dependent Jitter	--	0.15	UI pp	See Note 5.
UDJ	Deterministic jitter that is uncorrelated to the transmitted data	--	0.17	UI pp	
UDJ_LF	Low Frequency Uncorrelated Deterministic Jitter	--	0.04	UI pp	See Note 6.
DCD	Even-odd jitter associated with Duty-Cycle-Distortion	--	0.03	UI pp	
Y1	TX eye inner height (one-sided voltage opening of the differential signal)	140	--	mV	Measured for 1E6 UI. See Note 1, Note 2, and Figure 3-15.
Y2	TX eye outer height (one-sided voltage opening of the differential signal)	--	650	mV	Measured for 1E6 UI. See Note 1, Note 2, and Figure 3-15.

Receiver Tolerance Topology

- No channel use case
- Long passive cable use case
- **Challenge**: Imprecise calibration channel, incorrect stress cocktail, not achieving CTS calibration targets, short and long channel performance

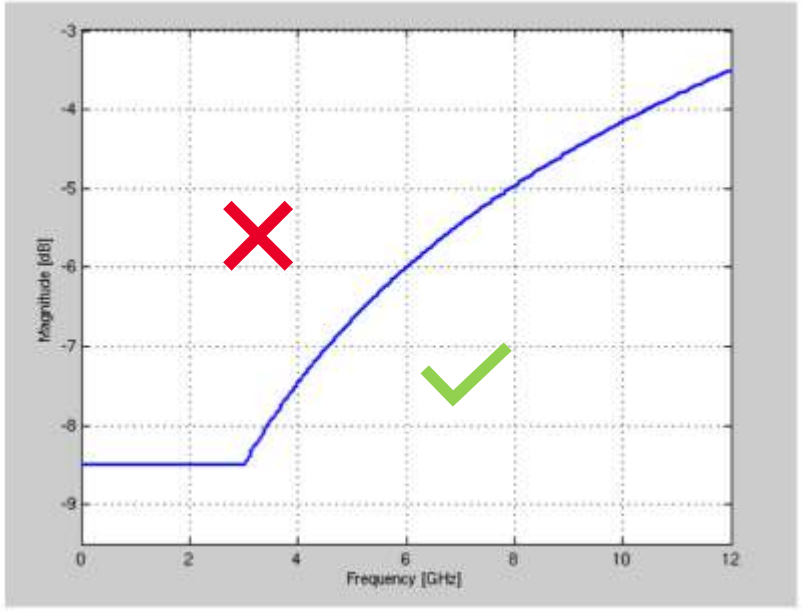


Return Loss

- TX and RX return loss
- Differential and Common Mode Return Loss
- **Challenge**: Very difficult to meet requirements, directly impacts TX and RX performance

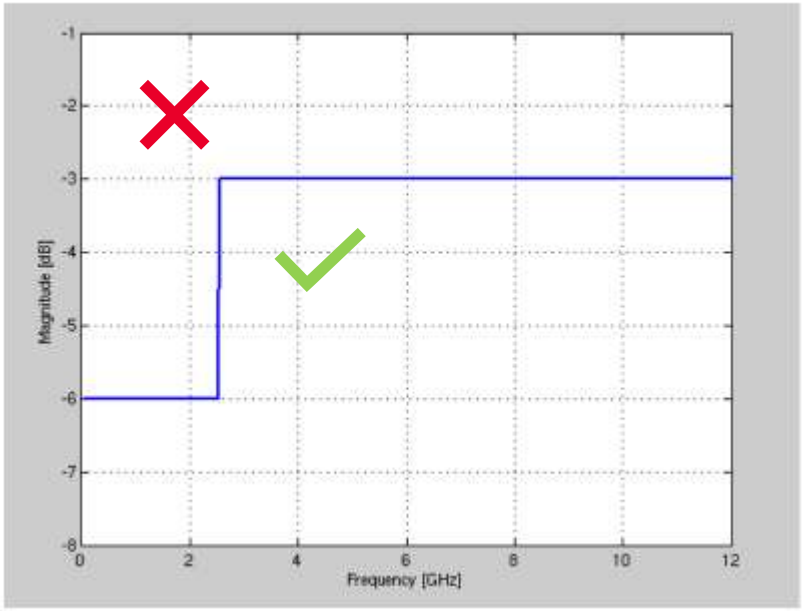
$$SDD22(f) = \begin{cases} -8.5 & 0.05 < f_{GHz} \leq 3 \\ -3.5 + 8.3 \cdot \log 10\left(\frac{f_{GHz}}{12}\right) & 3 < f_{GHz} \leq 12 \end{cases}$$

Figure 3-10. TX Differential Return Loss Mask



$$SCC22(f) = \begin{cases} -6 & 0.05 < f_{GHz} \leq 2.5 \\ -3 & 2.5 < f_{GHz} \leq 12 \end{cases}$$

Figure 3-11. TX Common-Mode Return Loss Mask

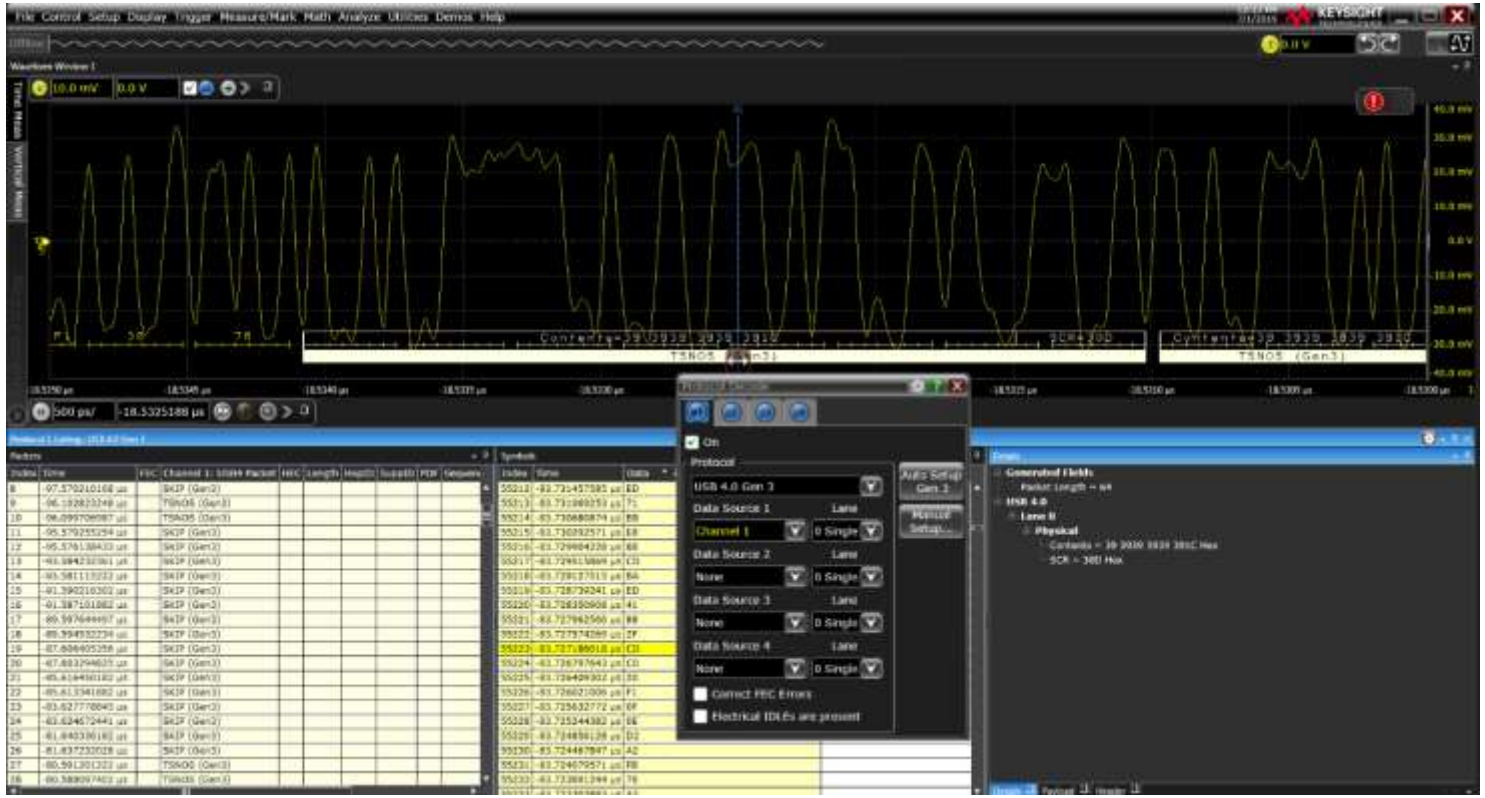


Current challenges between testing USB 3.2 x1 vs USB4

- Return Loss TX and RX
- Transmitter Equalization is not fixed and requires calibration
- Receiver Equalization is much more complex and requires optimization
- PHY bit rate doubles from 10 Gbps to 20 Gbps with significantly less margin
- Signaling on all 4 Type-C high-speed pairs
- Multiple bit rates: 10G, 20G and optionally 10.3125 and 20.625G
- Link management over the sideband channel
- Requirement for a passive, high-loss cable use case and short channel use case
- Retimer specific measurements
- New Jitter, Phase and Slew Rate Measurements
- Cross-talk Generation and Common Mode Interference
- Separate Jitter Cocktails for 10G/20G/TP2/TP3
- Built in Error Detector
- Link EQ Optimization prior to BER test
- Access to DUT status and error count over the sideband channel with Test Controller and USB4 Electrical Test Tool

Link Layer

- SBTX/SBRX in conjunction with high-speed TX/RX lanes are critical for link training
- **Challenge**: Incomplete view of Type-C signaling



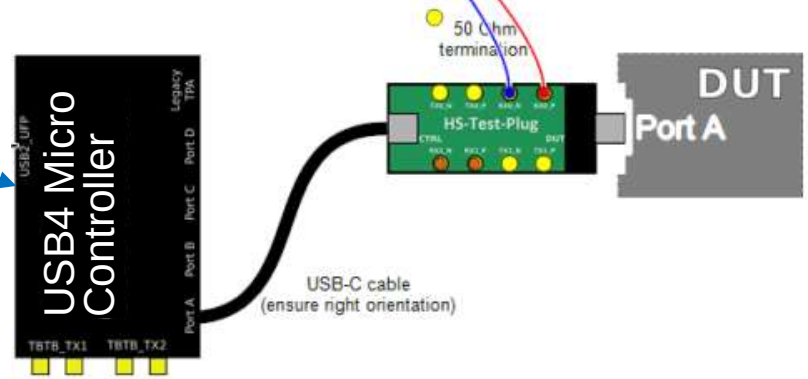
USB4 Automated Electrical Transmitter Test

D9040USBC USB4 Tx Automated Test Software

Keysight UXR/V/Z Series Oscilloscope

USB4ETT

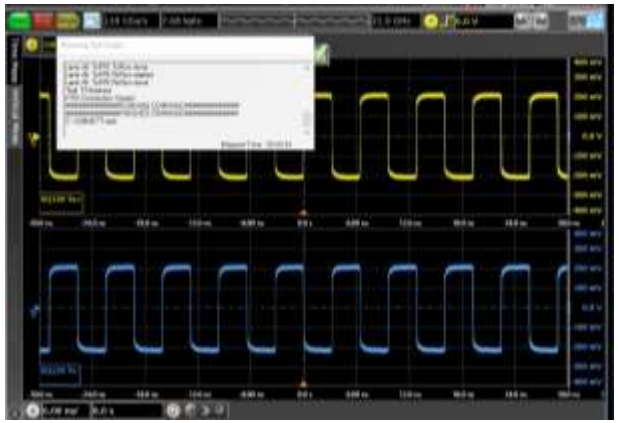
Control data rate, Tx EQ preset and test pattern



Measure both TP2, TP3+EQ Eye and Jitter (Calculate TP3+EQ waveform in oscilloscope)

Example USB4 Test Pattern Changes

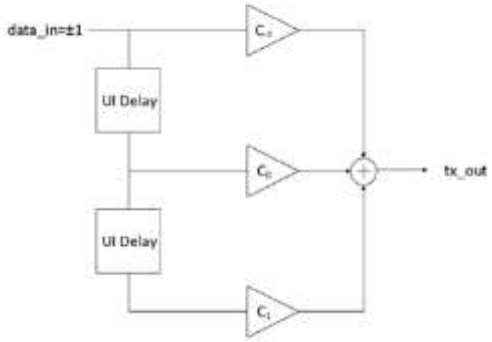
Rise/Fall Time: SQ128 (64 bit “1”, 64 bit “0”)



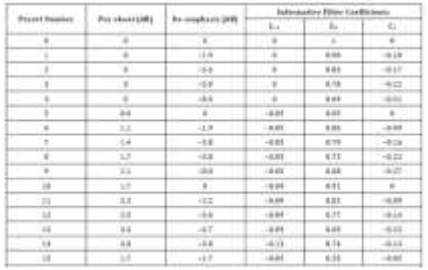
Eye Diagram Test: PRBS31

USB4 Automated Transmitter and Receiver Equalization Calibration

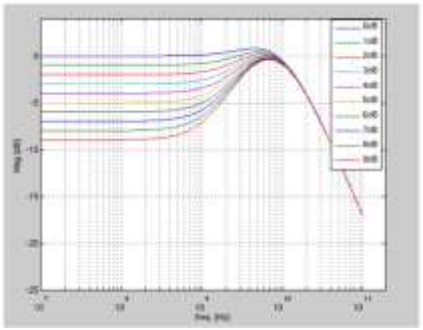
- Optimize TX FFE preset at TP3' → Select preset which minimizes DDJ (Data Dependent Jitter)
- Optimize RX CTLE DC gain + DFE at TP3 → Maximize the Eye Area (EW x EH)
- D9040USBC software automates these measurements and uses the optimal settings during tests



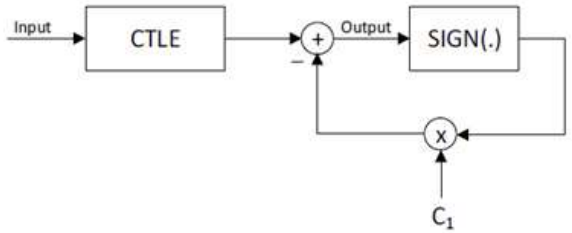
Transmitter Equalizer
3-tap FFE with 16 presets



D9040USBC USB4
Transmitter Test software

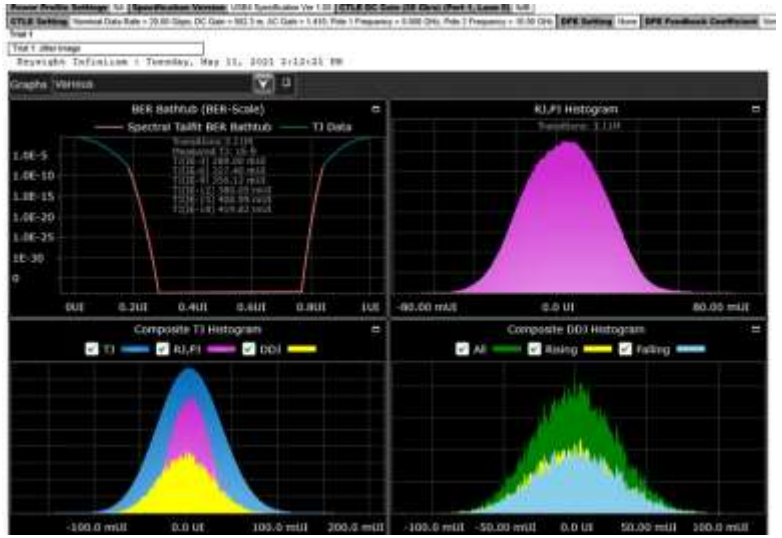


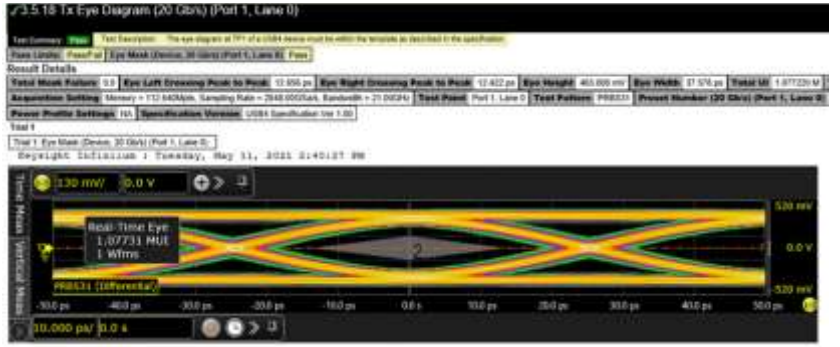
Receiver Equalizer
CTLE with 10 DC gain settings + DFE

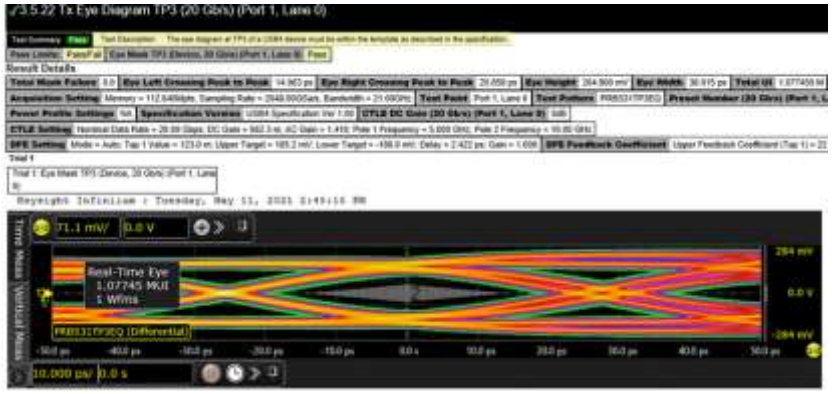


D9040USBC Automated Test Suite and Test Reports

- USB 4 Transmitter Tests
  - Device Transmitter Tests (Port 1)
    - Device Transmitter Tests (10.3125 GB/s)
      - Tx Rise/Fall Time
        - Tx Rise Time (Lane 0)
        - Tx Fall Time (Lane 0)
        - Tx Rise Time (Lane 1)
        - Tx Fall Time (Lane 1)
      - Tx Jitter
        - Tx Uncorrelated Jitter, Uncorrelated Deterministic Jitter
        - Tx Total Jitter
      - Tx Unit Interval and SSC Modulation
        - Tx Unit Interval and SSC Down Spread Modulation
        - Tx SSC Phase
      - Tx AC Common Mode Voltage
        - Tx AC Common Mode Voltage (Lane 0)
        - Tx AC Common Mode Voltage (Lane 1)
      - Tx Eye Diagram
        - Tx Eye Diagram (Lane 0)
        - Tx Eye Diagram (Lane 1)
        - Tx Eye Diagram TP3 (Lane 0)
        - Tx Eye Diagram TP3 (Lane 1)
      - Tx Lane to Lane Skew
        - Tx Lane to Lane Skew (Lane 0/Lane 1)
      - Tx Equalization
        - Tx Equalization Preshoot (Lane 0)
        - Tx Equalization Preshoot (Lane 1)
        - Tx Equalization Deemphasis (Lane 0)
        - Tx Equalization Deemphasis (Lane 1)
        - Tx Swing Preset 15 (Lane 0)
        - Tx Swing Preset 15 (Lane 1)
      - Tx Electrical Idle Voltage
        - Tx Electrical Idle Voltage (Lane 0)
        - Tx Electrical Idle Voltage (Lane 1)

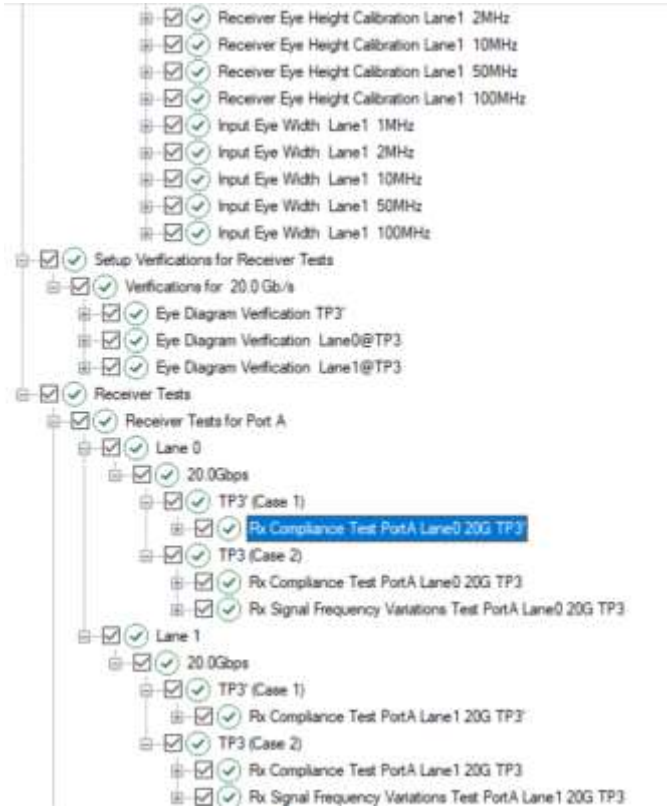


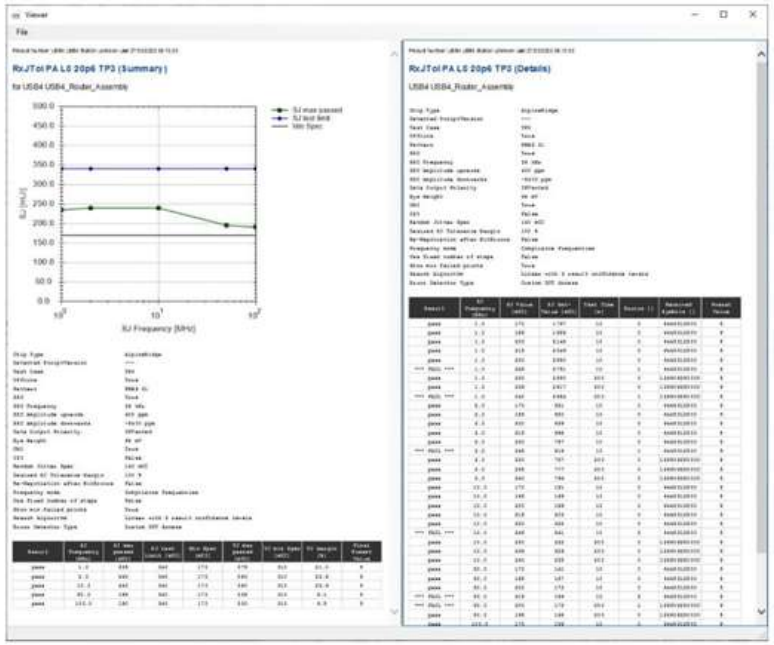




USB4 Automated Electrical Receiver Test

- Support both M8020A and M8040A High Performance J-BERT
- N5991U40A USB4 Receiver Test Software
- USB-IF USB4 Electrical Test Tool fully integrated



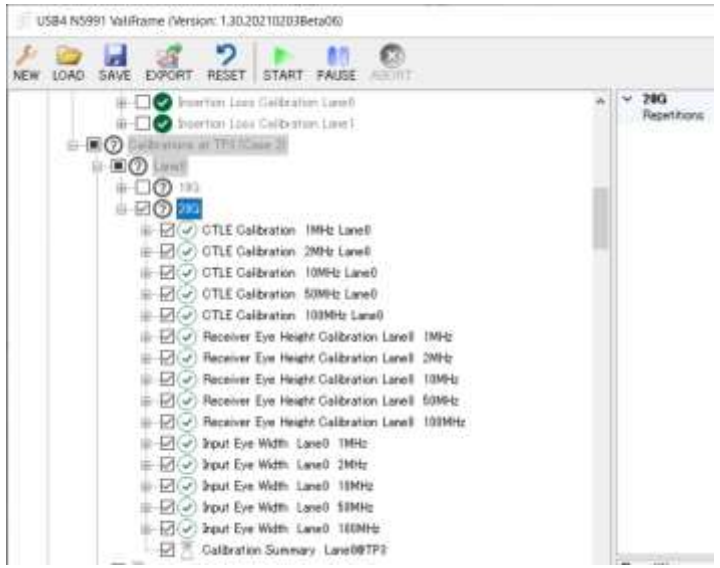


M8020A J-BERT + M8062A 32G front-end

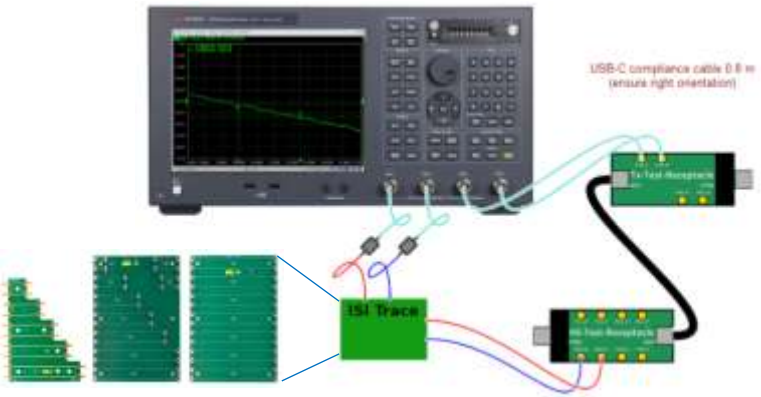
M8040A 32/64 Gbaud J-BERT

USB4 Automated Stress Signal Calibration

1 Case 1: Short Channel

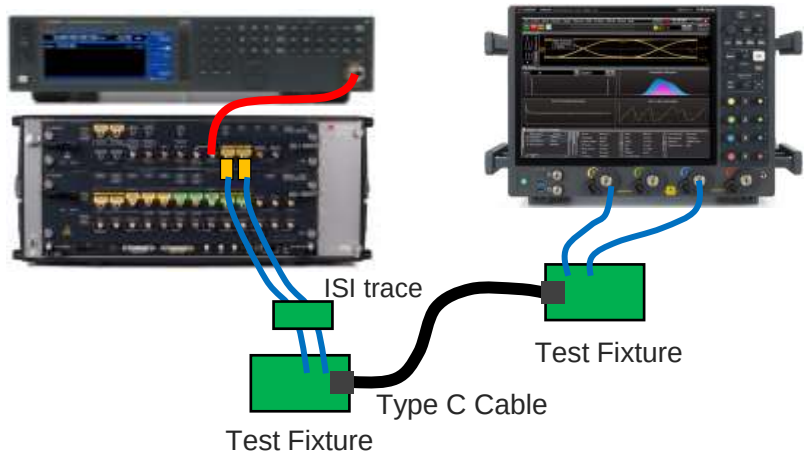


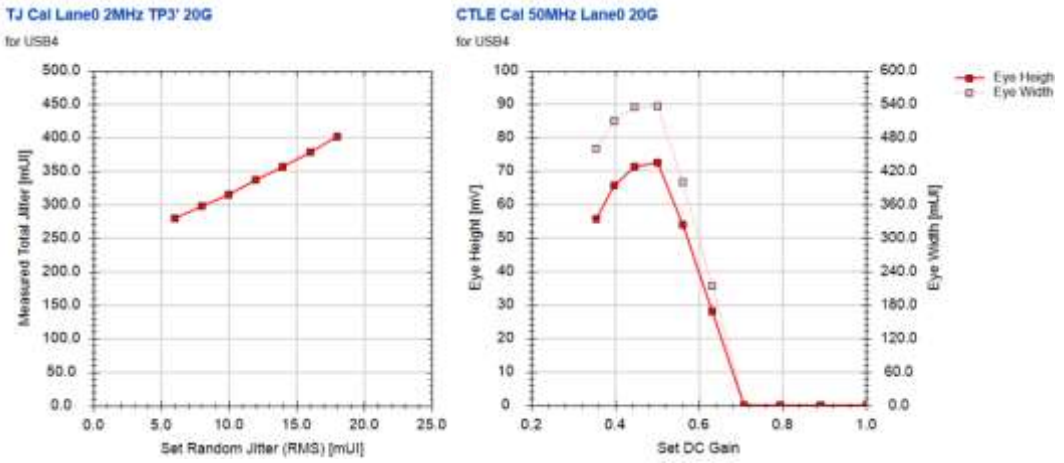
2 Long Channel Insertion Loss



N5991U40A
USB4 Receiver
Test Software

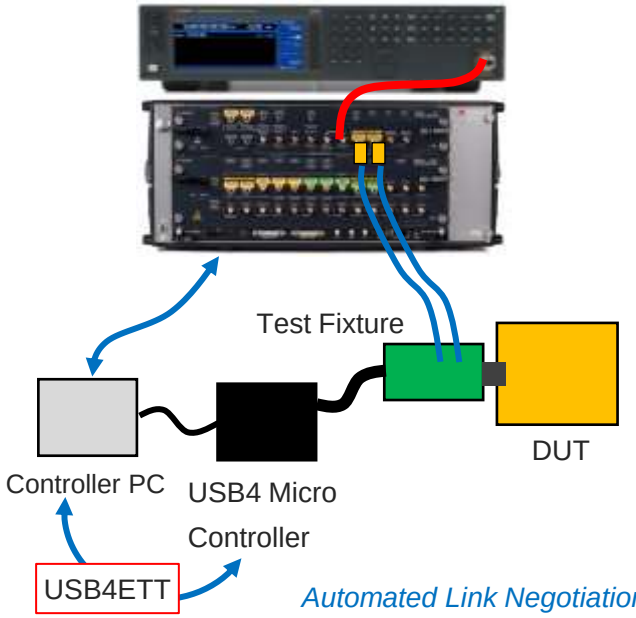
3 Case 2: Long Channel





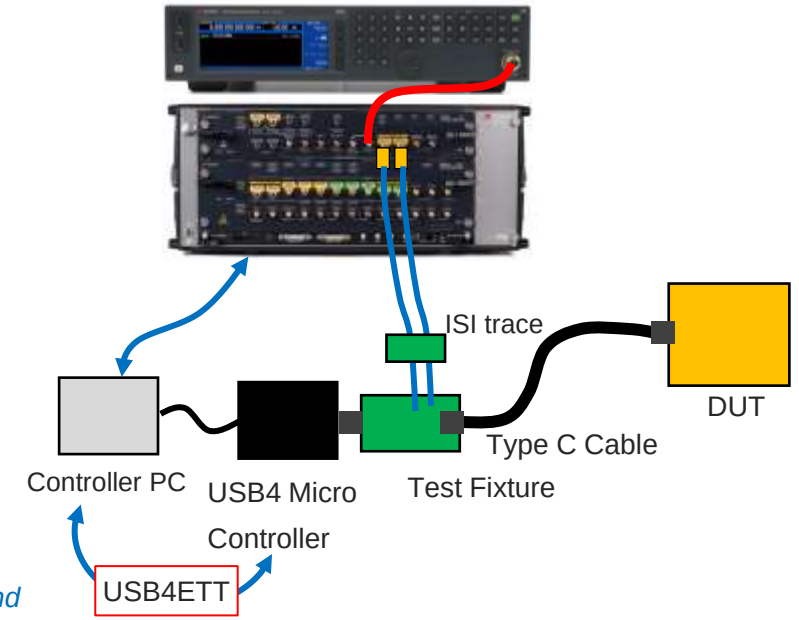
USB4 Automated Receiver BER Test

Case 1: Short Channel

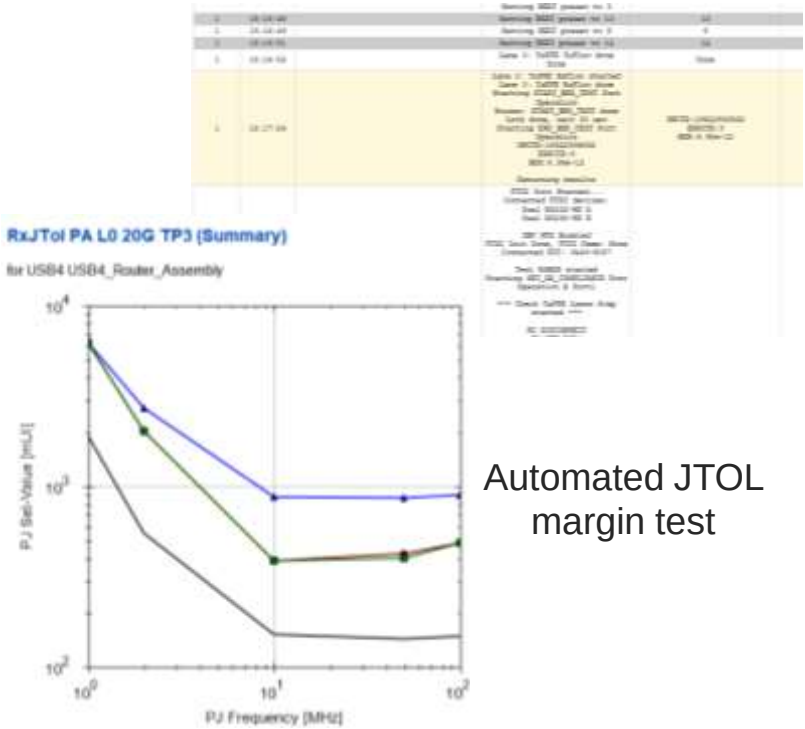


Automated Link Negotiation and Error Counter Check with the USB4 Electrical Test Tool

Case 2: Long Channel



Communication DUT ⇔ USB4ETT



Automated JTOL margin test

N5991U40A
USB4 Receiver Test Software

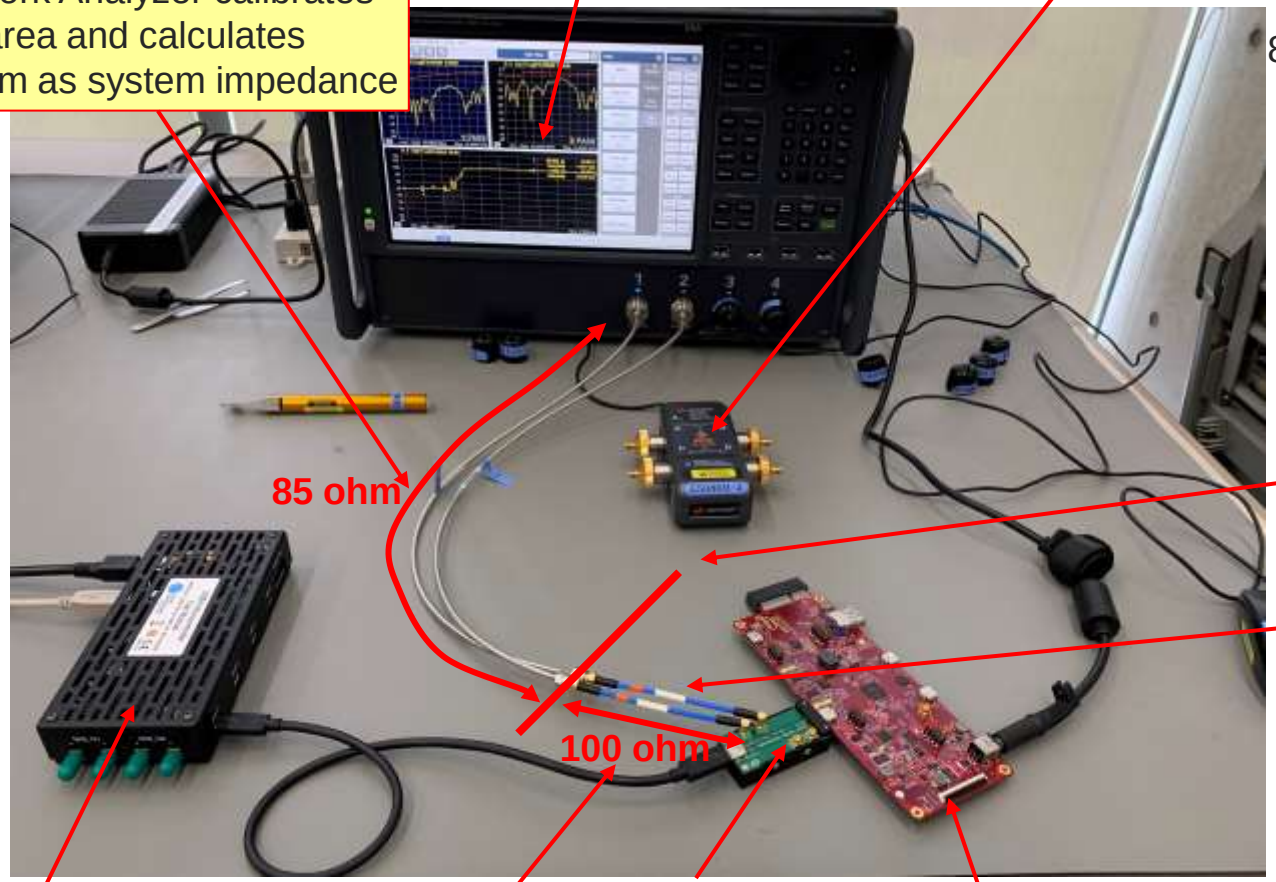
Detailed test report

Result	PJ Frequency [MHz]	AC CM Set Amplitude [mV]	PRBS Set Amplitude [mV]	RJ Set Value (RMS) [mUI]	PJ Set Value [mUI]	Final Preset Value	Error counter check 1st Run	passed negotiations	Component	Errors 1st Run	Symbol count 1st Run	Error counter check 2nd Run	Errors 2nd Run	Symbol count 2nd Run
pass	1	1001	1094	15.60	1907	0	Pass (3 of 3)	4	Router	0	124808413194	-	-	-
pass	2	1001	1067	16.10	551	12	Pass (3 of 3)	4	Router	0	124799686618	-	-	-
pass	10	1001	1158	16.30	152	12	Pass (3 of 3)	4	Router	0	124816857602	-	-	-
pass	50	1001	1160	16.30	144	0	Pass (3 of 3)	4	Router	0	124793236729	-	-	-
pass	100	1001	1165	10.60	196	12	Pass (3 of 3)	4	Router	0	124800063933	-	-	-

USB4 Return Loss Test

Test Setup Example

Network Analyzer calibrates this area and calculates 85ohm as system impedance



Remains extra reflection as 100ohm differential impedance

Calibration Plane

Calibration Plane

SMP-2.92mm Cable

SMP-2.92mm Cable

Test Fixture

Type C connector

USB4 DUT

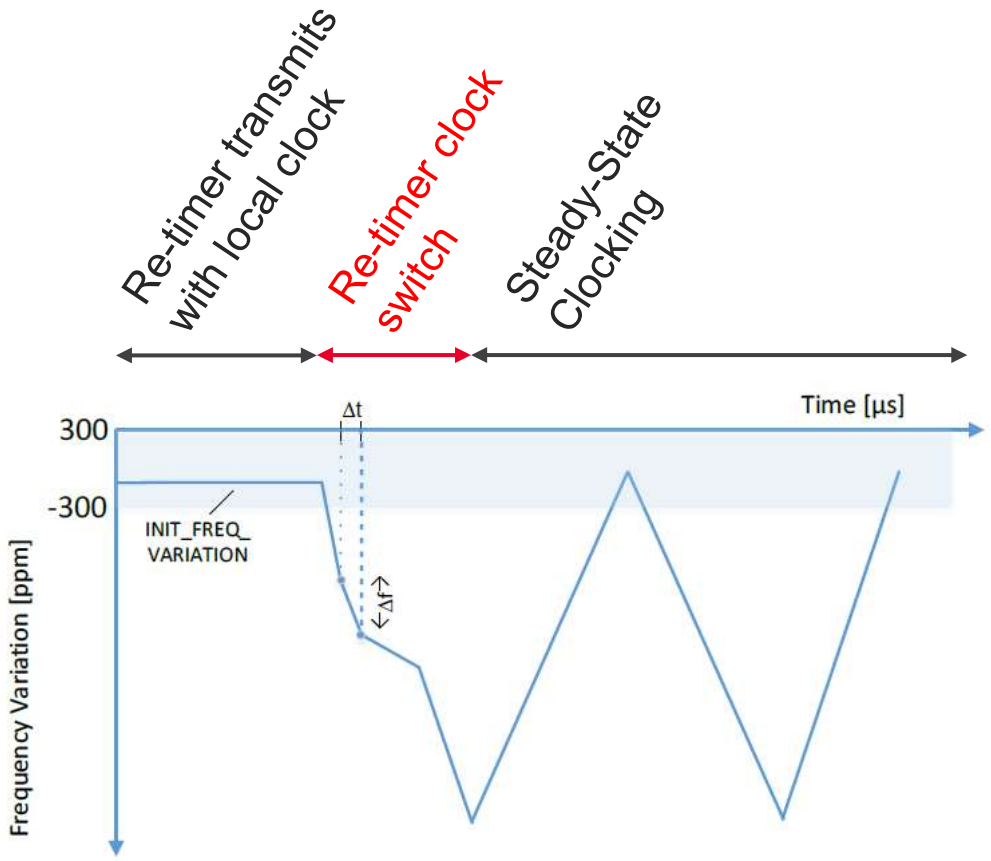
DUT's Source Termination

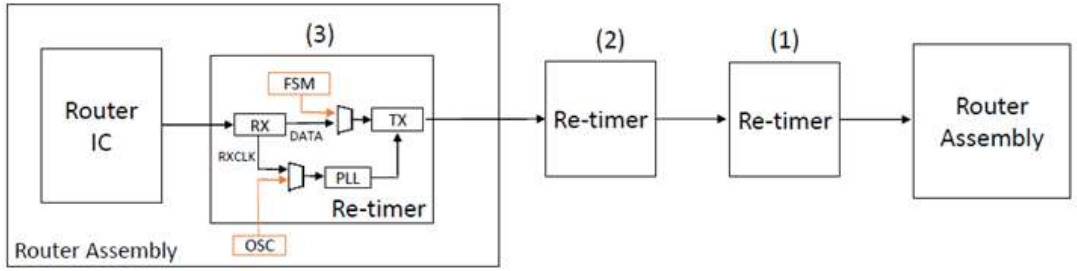
USB4 Tx Differential Impedance Example

Need to compensate this extra 100ohm area by "Gating" option of network analyzer

USB4 Signal Frequency Variation Test

USB4 Spec defines the Signal Frequency Variation Limit in Link Training for the System including Re-timers





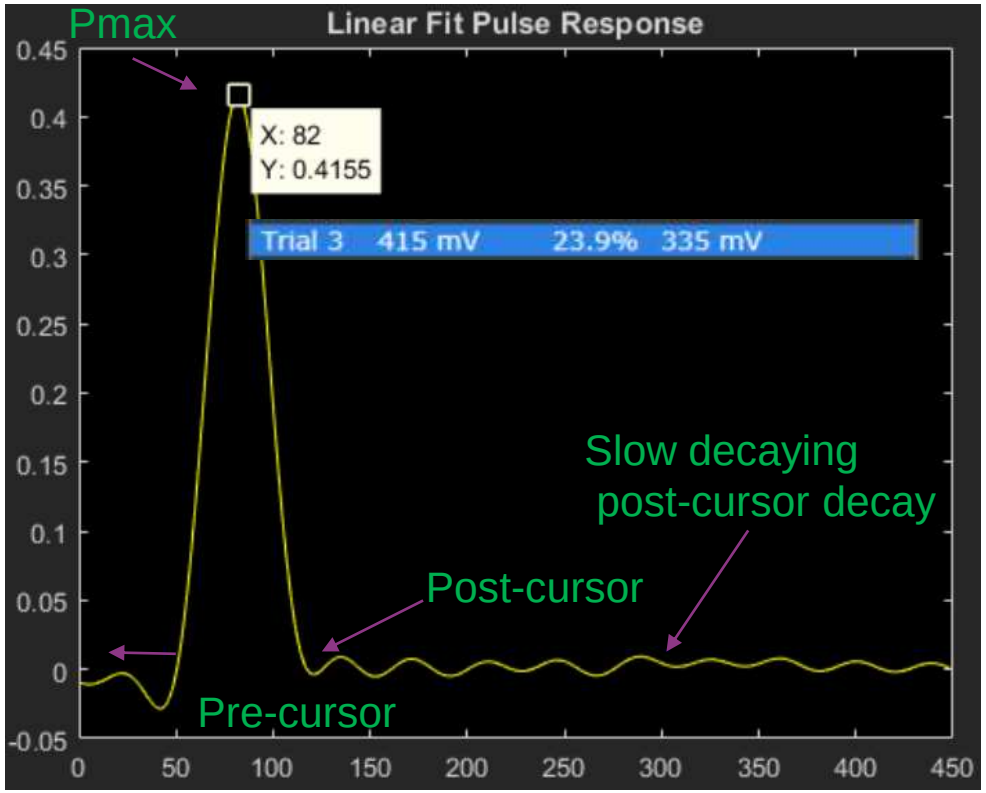
Signal Frequency Variation Test

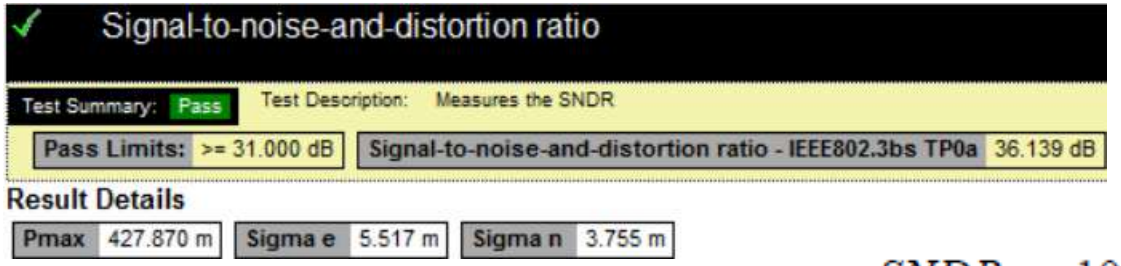
Tx Verify that a transmitter's frequency variation during link training falls within the limit.

Rx Verify that a receiver does not lose CDR lock when the frequency variation takes place.

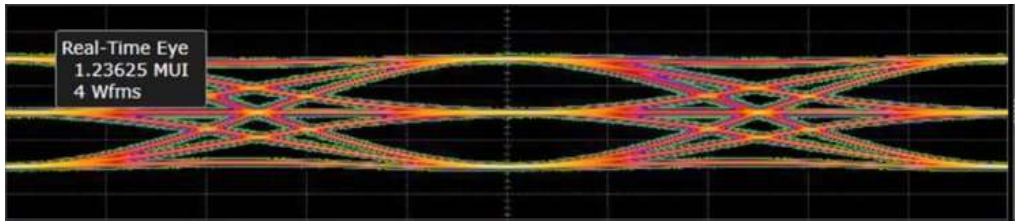
What happens after USB4 – PAM4?

- SNDR (Signal Noise Distortion Ratio)
  - LFPR (Linear Fit Pulse Response)
  - Sigma e
  - Sigma n
- R_{LM} (Level Separation Mismatch Ratio)
- TX ISI (Transmitter Output Residual ISI)
- PRBS13Q Patterns





$$SNDR = 10\log_{10}\left(\frac{p_{max}^2}{\sigma_e^2 + \sigma_n^2}\right)$$

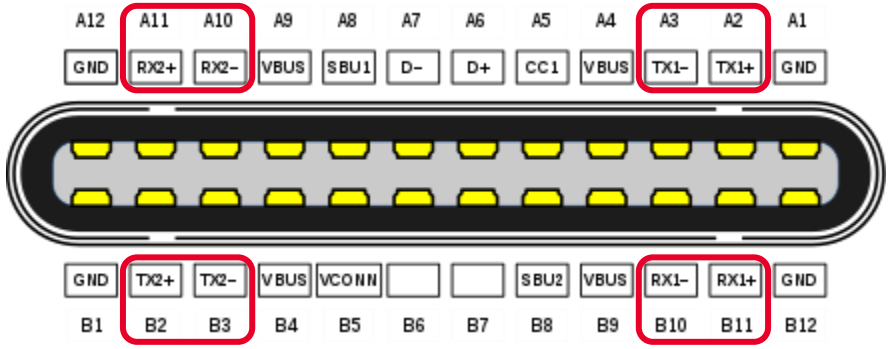


The Industry's Best Signal Integrity

- **10 bits ADC, 256 GSa/s**
- **Lowest noise**
  < 900 µV rms @ 110 GHz
  < 500 µV rms @ 70 GHz
  < 300 µV rms @ 33 GHz
- **Lowest intrinsic jitter**
  20 fs rms
- **Lowest inter-channel jitter**
  10 fs rms
- **Highest ENOB**
  > 5.0 bits @ 110 GHz
  > 5.4 bits @ 70 GHz
  > 5.9 bits @ 33 GHz

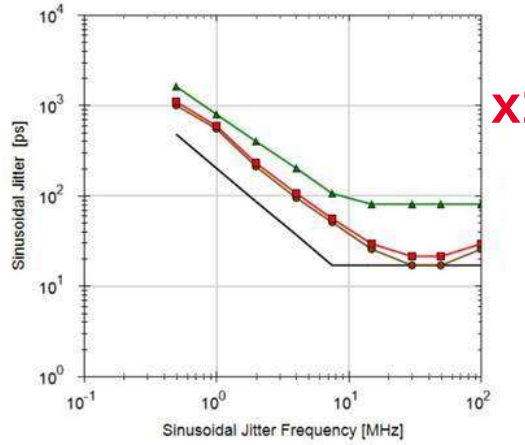
USB 3.2 Specification Update

- **New** dual lane (x2) mode over USB-C®
  - 5 Gb/s x2 → 10 Gb/s
  - 10 Gb/s x2 → 20 Gb/s
- The x2 capability is negotiated during the LBPM handshake
- All four high-speed lanes of the interface active
  - Additional crosstalk
  - Performance degradation

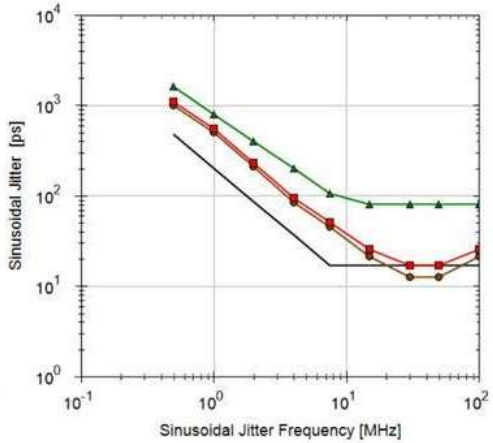


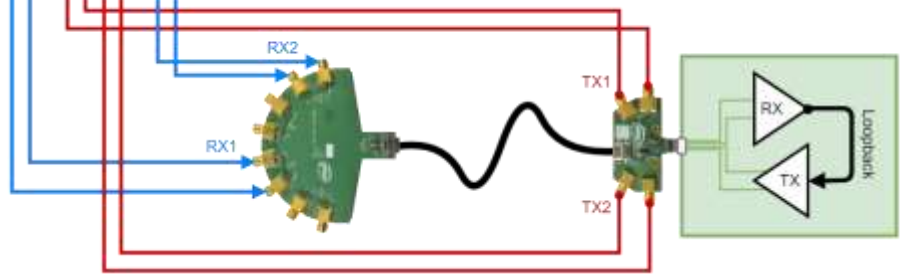
Best Known Method of x2 Receiver Testing

- Two Pattern Generators / Error Detectors
- Two independent RX paths fully calibrated
- Link Training in x2 mode
- Concurrent JTOL on both RX lanes
- USB-like traffic during test
- Test setup closest to operating condition



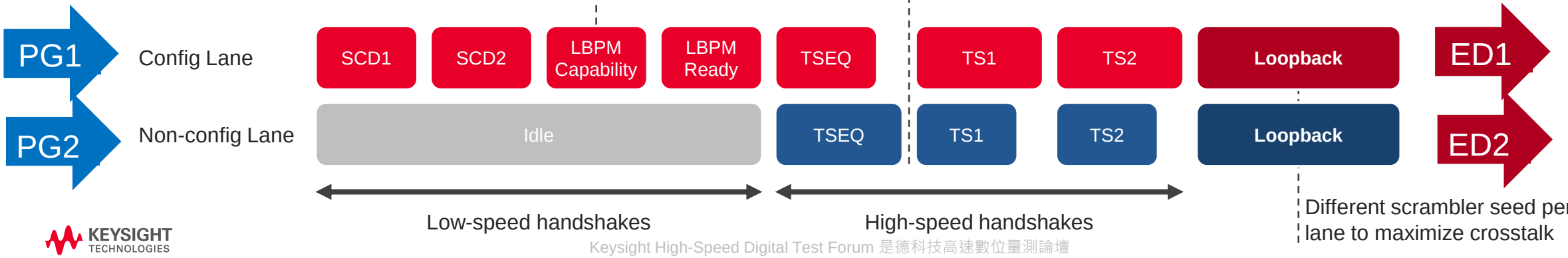
x1 vs x2





Negotiate link rate and bandwidth

Transition to next stage when both lanes are ready



Type-C Active Link Access, Automated Protocol Trigger Decode

N7019A Usage

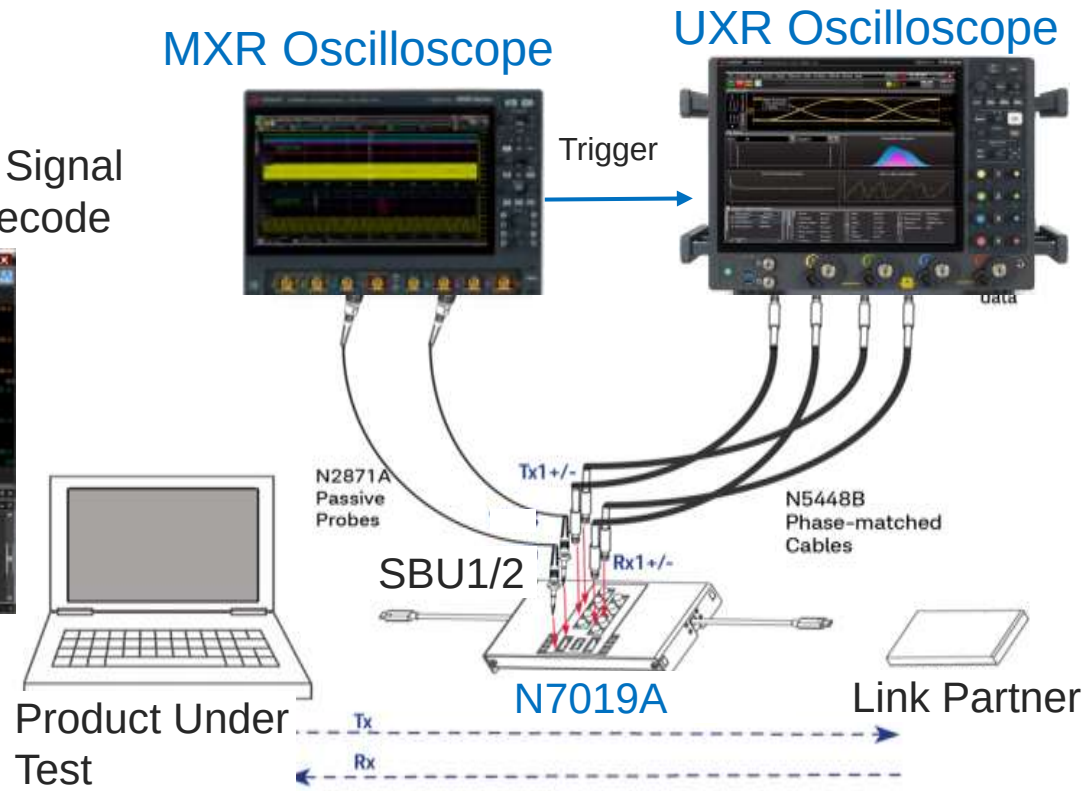
Provides access to all Type-C signals during an active link.

Signals include Vbus, USB 2.0, USB-PD, SBU1/2, and TX/RX up to maximum USB4 rate of 20 Gbps.

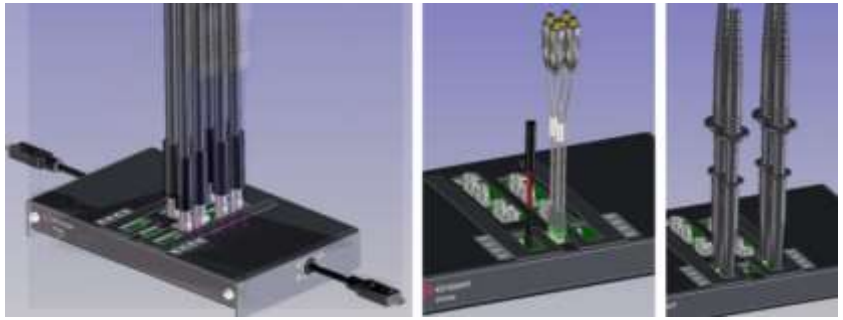
Works in conjunction with D9010USBP Keysight Protocol Trigger Decode solutions for USB-PD, eUSB2, USB 2.0, USB 3.2, USB4 and DP AUX.

New!

Measure Low Speed Signal (SBTX/SBRX) and Decode

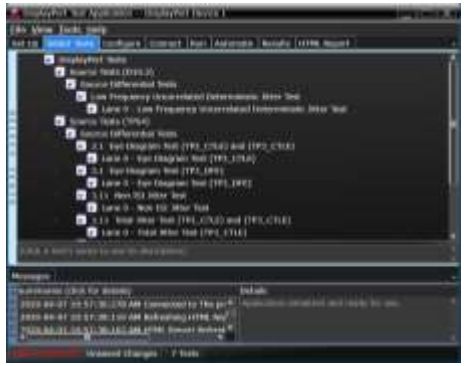


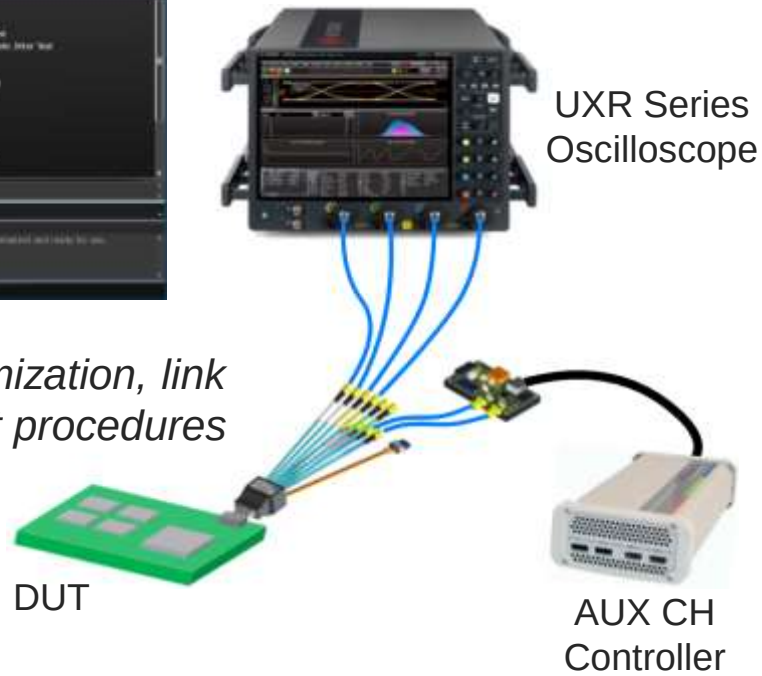
Measure High Speed Signal (TX1/RX1,TX2/RX2) and Decode



USB4 Related Solutions: DisplayPort UHBR

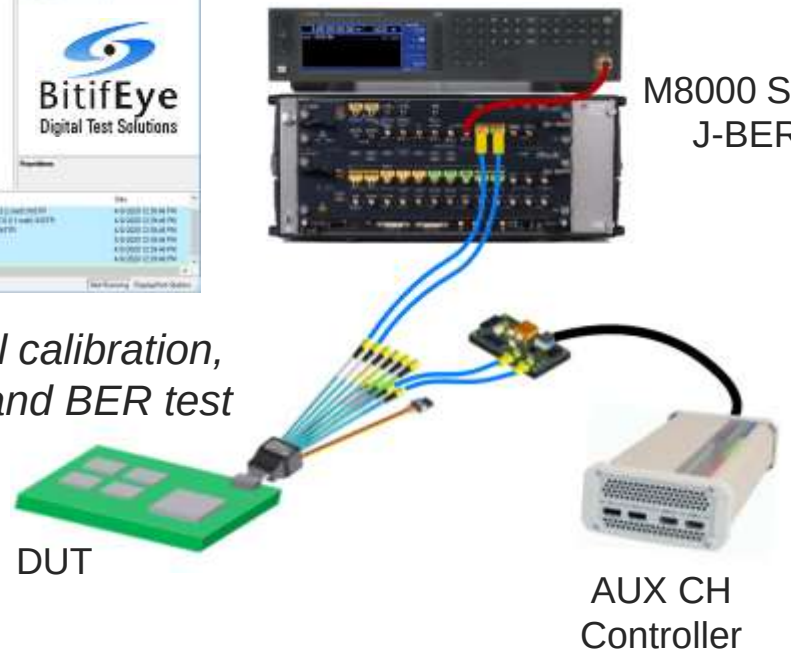
D9042DPPC
DisplayPort UHBR
Source Test Software





TX/RX EQ optimization, link training and test procedures

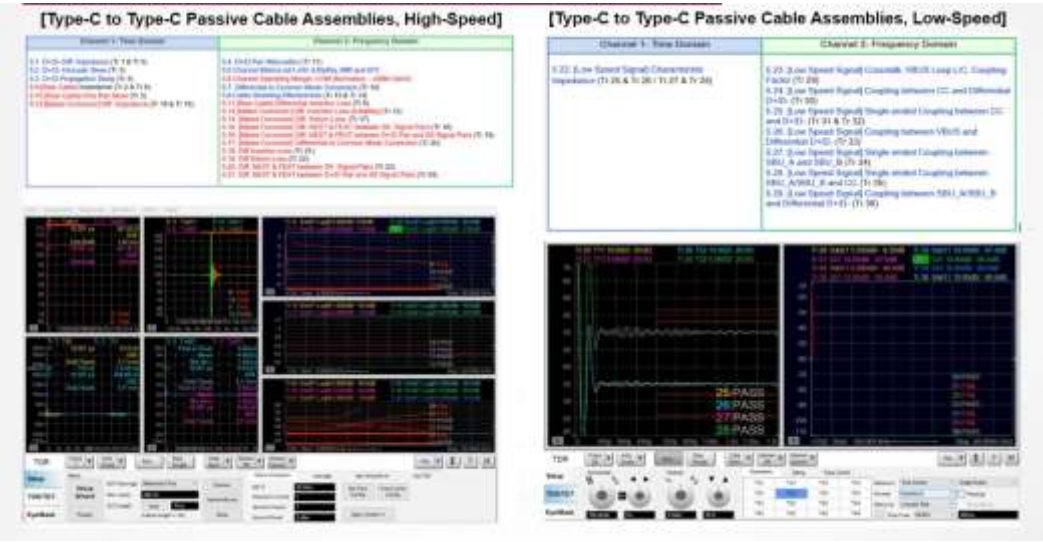
N5991DP2A
DisplayPort
Sink Test Software



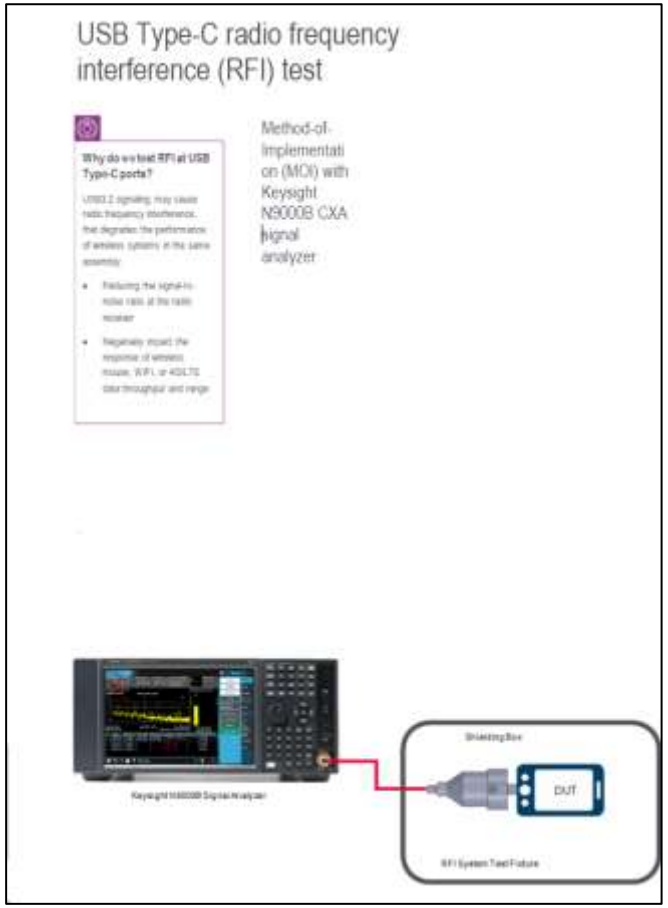
Stress signal calibration, link training and BER test

USB4 Related Solutions (cont.)

- USB 3.2 x2 (dual lane)
- Passive Cables for USB 3.2, USB4, DisplayPort
- LRD: Discrete, Embedded and Cable for USB 3.2, USB4, DP
- Retimer: Discrete, Embedded and Cable for USB 3.2, USB4, DP
- RFI



Technology Standards		Available MOI & State Files	
		Connectors and Cable Assemblies	Tx/Rx Hot TDR
USB	USB2.0	E5071C E5080B	N/A
	USB3.0	E5071C E5080B	N/A
	USB3.1	E5071C E5080B	N/A
	USB4.0 / USB Type-C	E5071C M937xA E5080B	E5071C E5080B
HDMI	HDMI 1.4b	E5071C	E5071C
	HDMI 2.0	E5071C	E5071C
	HDMI 2.1	E5071C M937xA	E5080B
SATA	v3.0	E5071C	E5071C
DisplayPort	v1.2b	E5071C	N/A
	v1.3	E5071C	N/A



HSD Cable Test Challenges

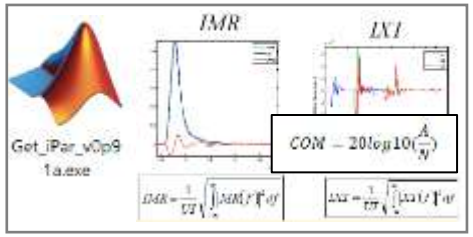
CURRENT MARKET SITUATION

Multiport

- Increase of device complexity that demand for multiport.
  - ➢ USB4/USB Type-C & DisplayPort required 20-ports
- True multi-port system is too expensive: >$300K for 20-ports PXI-VNA.
- No software automation for multiport, calibration and test execution are still manual.

Long Setup Time

- Calibration is complicated for custom switch solution.
- Compliance test procedures are tedious and prone to operation error.
  EG: USB4/USB Type-C passive cable required 44-sets of s4p for HS test manually, one cable sample could take 3-5 hours to complete.



Compliance Test Tool

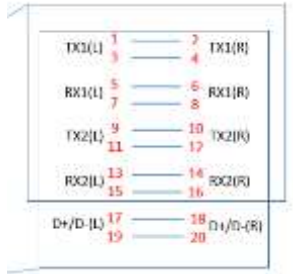
- USB-IF and VESA required compliance test tools to verify the integrated S-Parameters and COM results (Get_iPar and IntePar Matlab tools).
- Manual file configuration and setup to run the tools to determine final compliance results.

USB4/USB 3.2 Active/Passive Cable Compliance

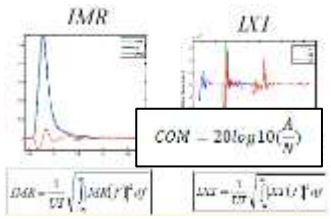
New COM test requirement for USB4-Gen3

Test Parameters	Passive Cable	Active Cable	Active Component
Channel Operating Margin (COM)	Normative	Normative	Not required
ILfitatNq	Normative	Normative	Not required
Integrated Multi-Reflection (IMR)	Informative	Normative	Not required
Integrated Return Loss (IRL)	Normative	Normative	Informative
Integrated Crosstalk (IXT for INEXT & IFEXT)	Normative	Not required	Informative
Integrated Crosstalk (IXT for IDDXT)	Normative	Not required	Not required

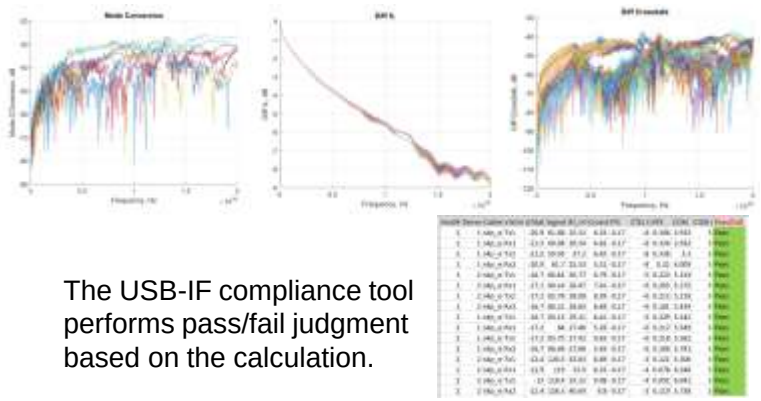
Manual steps to run Get_iPar tool = Time consuming (3-5 hours) and prone human error!



Touchstone S-parameter files (28x/44x *s4p) are saved and imported to run the tool.



COM, Integrated crosstalk (IXT), IRL, IMR etc are calculated from S-parameter files.



The USB-IF compliance tool performs pass/fail judgment based on the calculation.

* Same steps applied for USB Type-C Passive cable compliance test – Channel Metrics/COM.

Keysight Automated Test Solution

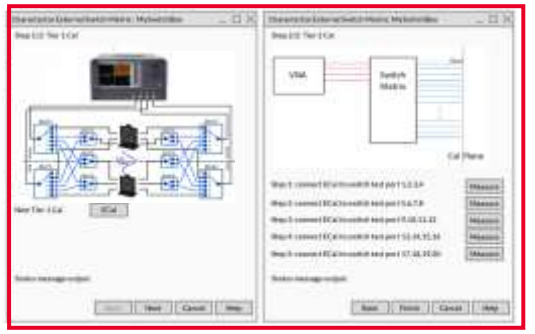
KEY FEATURES

- Affordable price compared to true multiport PXI-VNA system.
- Fully automated switch matrix control without any cable/port reconnection.
- Auto calibration and de-embedding wizards.
- PathWave TAP based compliance software for automation and test sequencing.
- Comprehensive HTML reports with result table and waveform diagrams.
- Supports Keysight E5080B, Streamline USB/TBT Series VNA and PXI-VNA.
- Compliance test by HSD module:
  - USB Type-C (First Release)
  - DisplayPort
  - HDMI

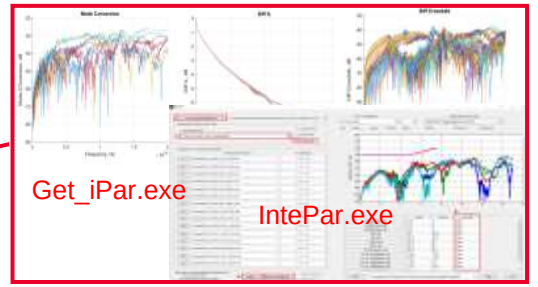
Hardware solution are available for order NOW!

Keysight Automated Cable Test

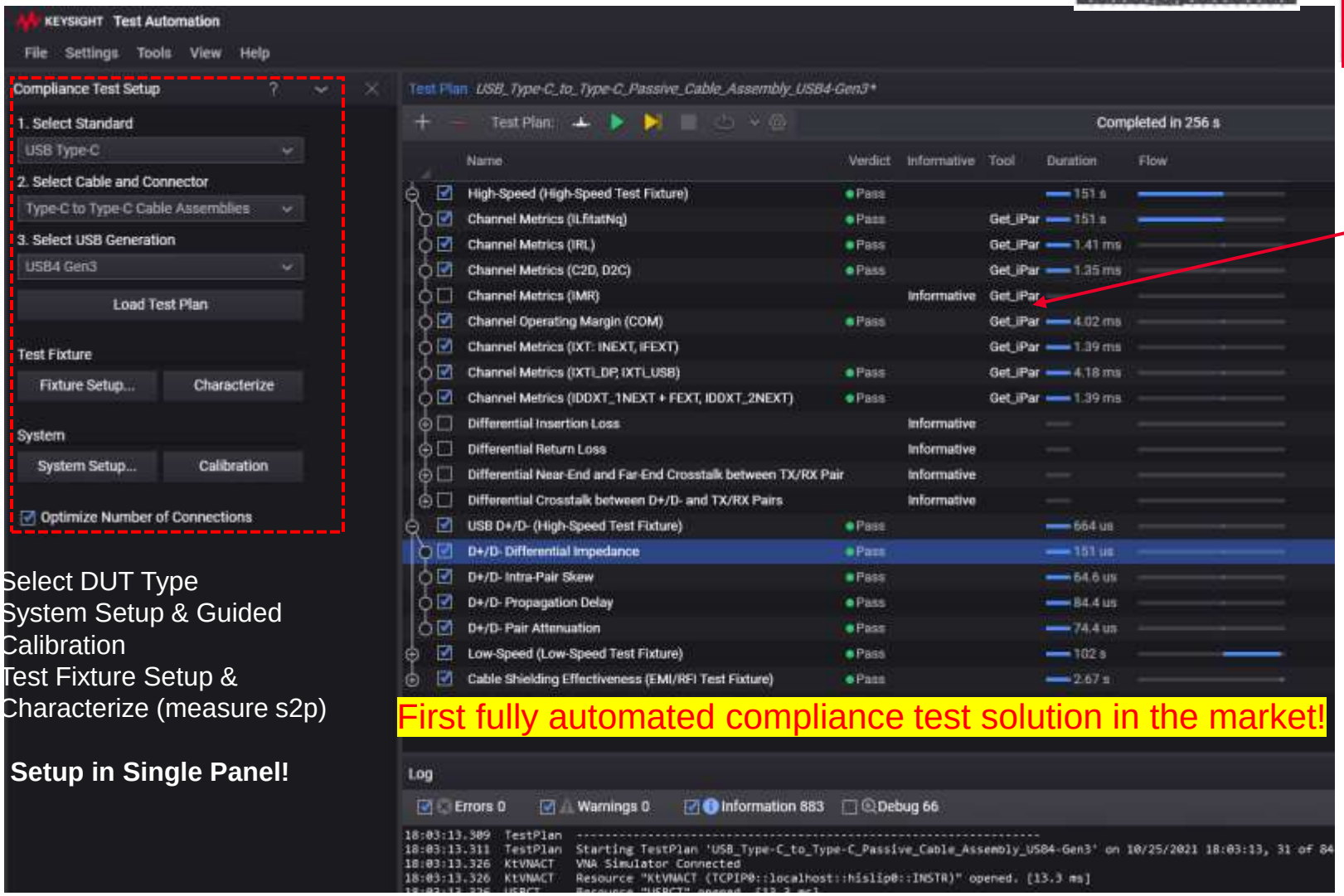
KEY FEATURES PREVIEW



Guided connection and setup diagram



Auto-compliance tool in single platform



Select DUT Type
System Setup & Guided Calibration
Test Fixture Setup & Characterize (measure s2p)

Setup in Single Panel!

First fully automated compliance test solution in the market!

Real-time trouble-shooting

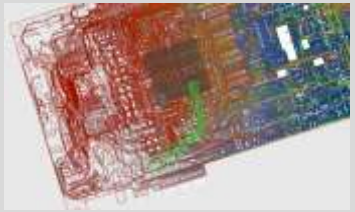
HTML/CSV test report

Keysight Type-C Solutions Matrix

Design Simulation, Protocol Decode, Live Link Debug, USB-PD, RF, Channel Characterization, SBU, USB, Thunderbolt, DisplayPort

Physical Layer System Simulation

ADS Design Software



SIPro/PIPro

Simulation to measurement correlation

Transmitter Test Active Cable Test

Automated Standards Test Software

UXR Infiniium Scope <1mV RMS <25fs RMS

TX Test Fixture

Interconnect Test Return Loss Test

E5080B ENA with S96011A Enhanced TDR software

Cable/Connector Test Fixture

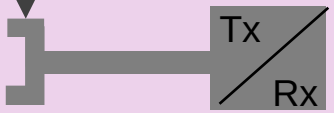
Active/Passive Cable

Receiver Test Active Cable Test

Automated Standards Test Software

M8000 J-BERT <200fs RMS

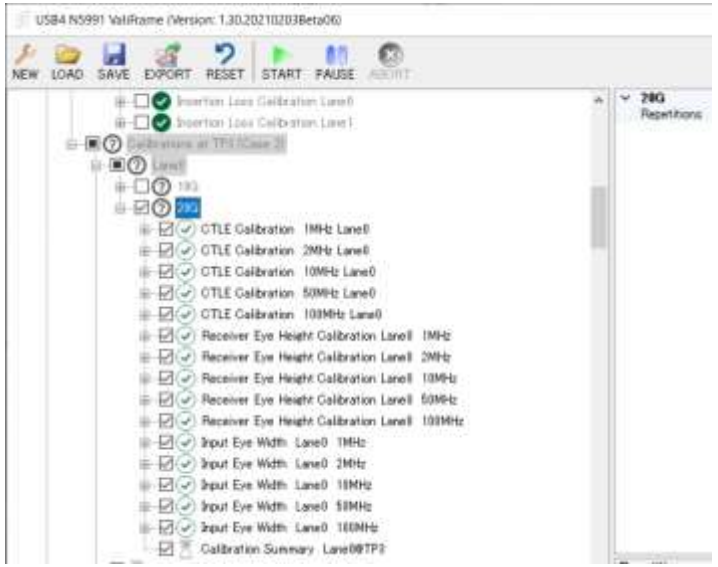
RX Test fixture



Best Solution for USB4 and Beyond

- UXR: best signal integrity, lowest noise, same argument as PCIe
  - Supports next-generation technologies with multi-level signaling
  - Most accurate jitter and noise analysis tools
  - Advanced equalization and math functions
- RX test solution supports M8020A and M8040A
  - Lowest intrinsic RJ in the market
  - Multi-tap FFE for accurate equalization
  - The M8040A supports next-generation technologies with multi-level signaling

- Keysight has been used to certify the vast majority of shipped TBT3/USB4 products
- TX and RX test automation software
  - SigTest and USB4 Electrical Test Tool (USB4ETT) fully integrated
  - Easy configuration and operation
  - Unattended test execution



- Unique product N7019A with D9010USBP protocol decode software
  - Examine all 24 pins of the USB Type-C interface: high-speed lanes, SBU, CC, power, etc.
  - Debug link bring-up issues on a live link between two products
  - Covers the entire USB Type-C ecosystem: USB PD, USB 2.0, USB 3.2, USB4, DP1.4a, DP2.1 (coming)


KEYSIGHT
TECHNOLOGIES