

Next Gen Development in Type-C Ecosystem and USB4/TBT4 Update Include LRD Active Cable

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2021.12

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Agenda

- Technology Overview
- Testing Challenges
- Lessons Learned
- Solutions Summary

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Diagrams courtesy of USB Implementers Forum

USB4 Technology Overview

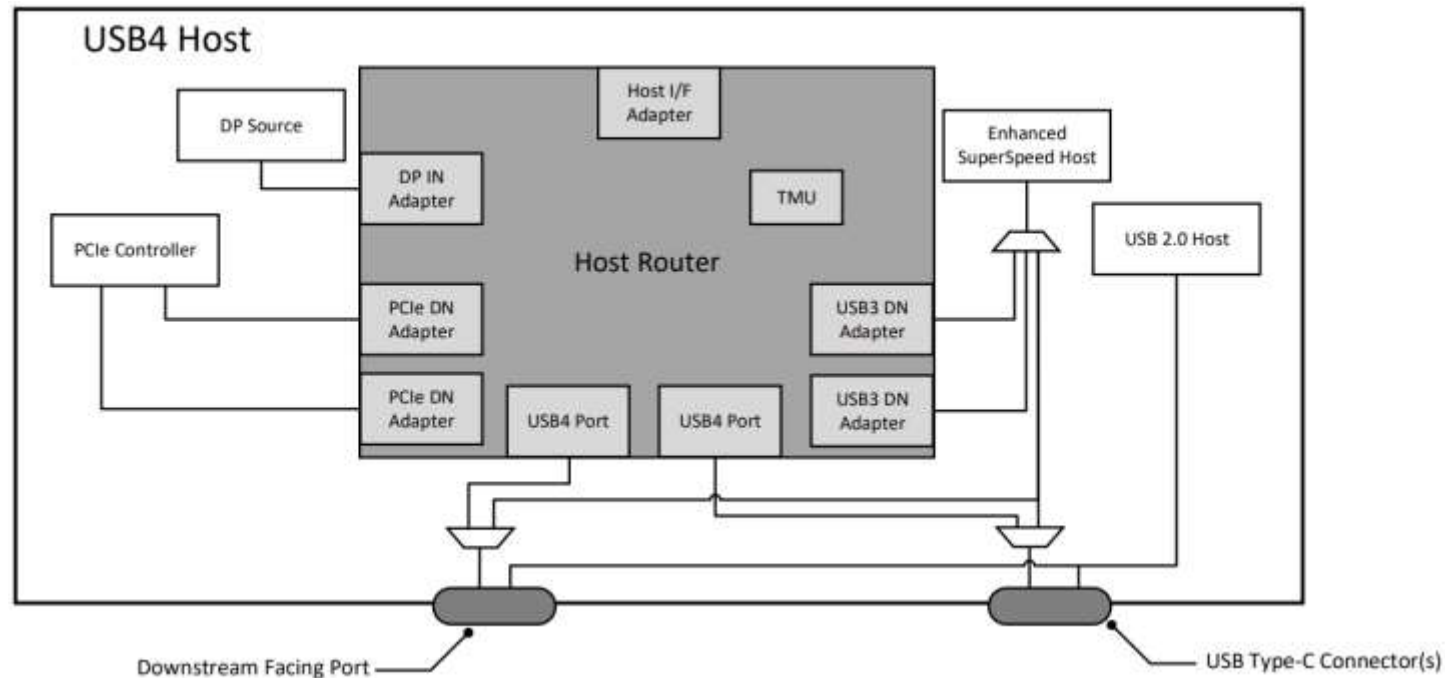
- Announced by USB-IF in March 2019
- Spec released September 2019
- Based on the Thunderbolt 3 protocol
- Uses the Type-C connector
- Two 20 Gb/s PHY lanes bonded into one logical 40 Gb/s link
- CTS is available but potential future updates to test methodology
- One Spec and Electrical CTS for USB4/TBT4/TBT3
- Numerous USB4 Products shipping and available on the market
- Driven by 5G adoption

Universal Serial Bus 4 (USB4™)
Specification

**Universal Serial Bus 4 (USB Type-C)
Electrical Compliance Test Specification**

Architecture Overview

- Must test for USB4 with and without retimers
- USB 3.2, USB 2.0, DisplayPort, Thunderbolt compatibility
- **Challenge:** Same port, different standards, similar speeds, different cable losses.



Insertion Loss Budget

- Insertion Loss Budget is the foundation for Silicon or End Products
- USB 3.2 Gen 2 10G has different loss budget
- **Challenge:** Long channel and short/no channel use cases and multiple bit rates and standards over same physical port

3.2 USB4 Ecosystem

3.2.1 Insertion-Loss Considerations (Informative)

The insertion-loss of the physical media is a key factor for facilitating USB4 electrical compliance. It is recommended that a Router Assembly limit the total insertion-loss from the USB Type-C® receptacle to the USB4 transceiver as follows:

- The total insertion-loss for a Router Assembly supporting Gen 2 is less than or equal to 5.5 dB at 5 GHz, including the receptacle tongue, the PCB trace, the integrated circuit's package and die load.
- The total insertion-loss for a Router Assembly that supports Gen 3 is less than or equal to 7.5 dB at 10 GHz, including the receptacle tongue, the PCB trace, the integrated circuit's package and die load.

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Version 1.0
August, 2019

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Universal Serial Bus 4
Specification

For a Captive Device that employs a passive attached cable, it is recommended that the device limit the total insertion-loss from the USB Type-C plug to the USB4 transceiver as follows:

- The total insertion-loss for a Captive Device supporting Gen 2 is less than or equal to 17.5 dB at 5 GHz, including the plug, the cable, the on-board connector, the PCB trace, the integrated circuit's package, and die load.
- The total insertion-loss for a Captive Device supporting Gen 3 is less than or equal to 15 dB at 10 GHz, including the plug, the cable, the on-board connector, the PCB trace, the integrated circuit's package, and die load.

Data Rate	Host	Connector	Cable	Connector	Device
5G	10dB	Std A	7.5dB	Std B	2.5dB
5G	10dB	Std A	3.5dB	Micro B	6.5dB
5G	6.5dB	C	7dB	C	6.5dB
5G	10dB	Std A	3.5dB	C	6.5dB
5G	6.5dB	C	4dB	Std B	2.5dB
5G	6.5dB	C	4dB	Micro B	6.5dB
10G	8.5dB	Std A	6dB	Std B	8.5dB
10G	8.5dB	Std A	6dB	Micro B	8.5dB
10G	8.5dB	Std A	6dB	C	8.5dB
10G	8.5dB	C	6dB	Std B	8.5dB
10G	8.5dB	C	6dB	Micro B	8.5dB
10G	8.5dB	C	6dB	C	8.5dB

Speed	Total Budget (dB)	Host (dB)	Cable (dB)	Device (dB)
Gen2 (10G)	23	5.5	12	5.5
Gen3 (20G)	22.5	7.5	7.5	7.5

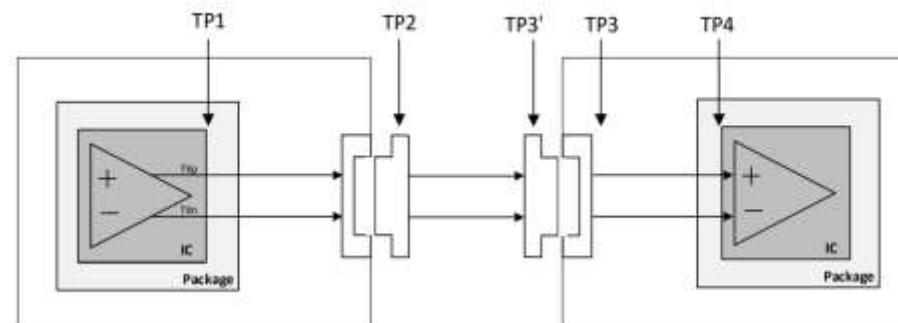
Electrical Compliance Test Points

- TP definition has no set rules
- For USB4, what are the specific test points for TX and RX, short channel and long channel?
- **Challenge:** Imprecise TP understanding invalidates testing

Table 3-2. Electrical Compliance Test Points

Test Point	Description	Comments
TP1	Transmitter IC output	Not used for electrical testing.
TP2	Transmitter port connector output	Measured at the plug side of the connector.
TP3	Receiver port connector output	Measured at the receptacle side of the connector. All the measurements at this point shall be done while applying reference equalization function.
TP3'	Receiver port connector input	Measured at the plug side of the connector.
TP4	Receiver IC input	Not used for electrical testing.

Figure 3-2. Compliance Points Definition



Transmitter Specifications (Short/Long Channel Use Case)

- Traditional voltage, eye, SSC, 10ps min rise/fall times
- Traditional UI, TJ, DDJ jitter decomposition
- **Challenge:** New uncorrelated jitter, phase, retimer measurements, short and long channel use case

Table 3-3. Transmitter Specifications Applied for All Speeds (at TP2)

Symbol	Description	Min	Max	Units	Conditions
RL_DIFF	Differential Return Loss, 0.05-10GHz	--	See Section 3.6.1.2	dB	
RL_COMM	Common Mode Return Loss, 0.05 - 10GHz	--	See Section 3.6.1.2	dB	
TX_RQ	Transmitter Equalization Setting	--	See Section 3.6.1.4		
SSC_DOWN_SPREAD_RANGE	Dynamic range of SSC down-spreading during steady-state	0.4	0.5	%	See Note 3, Note 4, and Figure 3-9.
SSC_DOWN_SPREAD_RATE	SSC down-spreading modulation rate during steady-state	30	33	KHz	See Note 4 and Figure 3-9.
SSC_PHASE_DEVIATION	Phase jitter associated with the SSC modulation during steady-state	2.5	33	ns pp	See Note 1, Note 4, and Figure 3-9.
SSC_SLEW_RATE	SSC frequency slew rate (df/dt) during steady-state	--	1250	ppm/ps	See Note 2, Note 4, and Figure 3-9.
TX_FREQ_VARIATIONS_TRAINING	TX frequency variation during Link training, before obtaining steady-state	--	See Section 3.6.1.1	ppm	See Note 4.
LANE_TO_LANE_SKEW	Skew between dual transmit signals of the same USB4 Port	--	26	ns	See Note 5.
RISE_FALL_TIME	TX rise/fall time measured between 20-80% levels	10	--	ps	Test pattern shall be SQ12B (see Table 8-56).
V_EYE_SIZE	Peak voltage during transmit electrical idle (one-sided voltage opening of the differential signal)	--	20	mV	See Note 6.
V_TX_DC_AC_COMM	Instantaneous DC+AC voltage at the connector side of the AC coupling capacitors	-0.3 (min1) -0.3 (min2)	1.0	V	See Note 7.

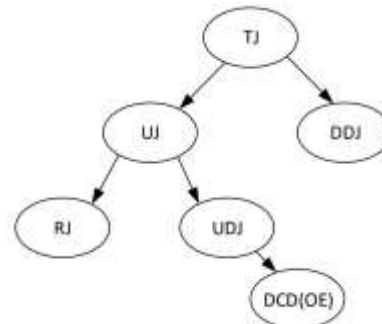


Figure 3-15. TX Mask Notations

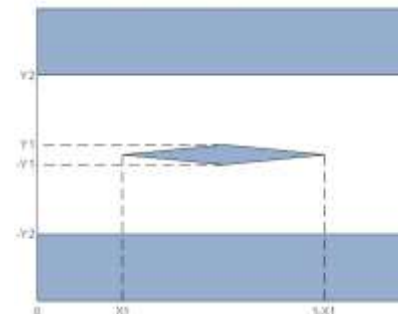


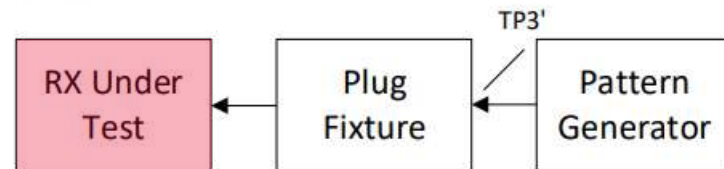
Table 3-6. Gen 2 Transmitter Specifications at TP2

Symbol	Description	Min	Max	Units	Comments
UI	Minimum Unit Interval	99.97	100.03	ps	The minimum UI value corresponds to the Link baseline speed of 10.0 Gbps with an uncertainty range of -300 ppm to 300 ppm. See Note 4.
AC_CM	TX AC Common Mode voltage	--	100	mV pp	
TJ	Total Jitter	--	0.38	UI pp	See Note 2 and Note 3.
UJ	Sum of uncorrelated DJ and RJ components (all jitter components except for DDJ)	--	0.31	UI pp	See Note 2.
DDJ	Data-Dependent Jitter	--	0.15	UI pp	See Note 5.
UDJ	Deterministic jitter that is uncorrelated to the transmitted data	--	0.17	UI pp	
UDJ_LF	Low Frequency Uncorrelated Deterministic Jitter	--	0.04	UI pp	See Note 6.
DCD	Even-odd jitter associated with Duty-Cycle-Distortion	--	0.03	UI pp	
Y1	TX eye inner height (one-sided voltage opening of the differential signal)	140	--	mV	Measured for 1E6 UI. See Note 1, Note 2, and Figure 3-15.
Y2	TX eye outer height (one-sided voltage opening of the differential signal)	--	650	mV	Measured for 1E6 UI. See Note 1, Note 2, and Figure 3-15.

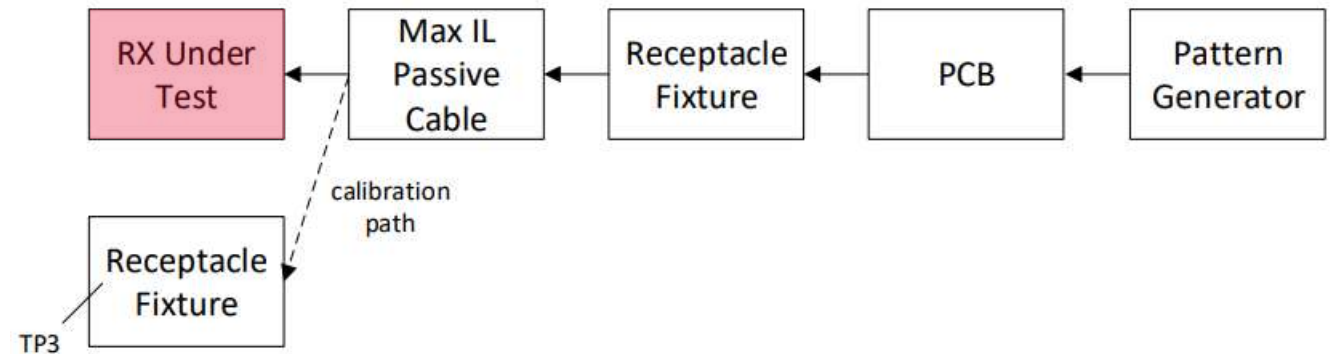
Receiver Tolerance Topology

- No channel use case
- Long passive cable use case
- **Challenge:** Imprecise calibration channel, incorrect stress cocktail, not achieving CTS calibration targets, short and long channel performance

Case 1:



Case 2:

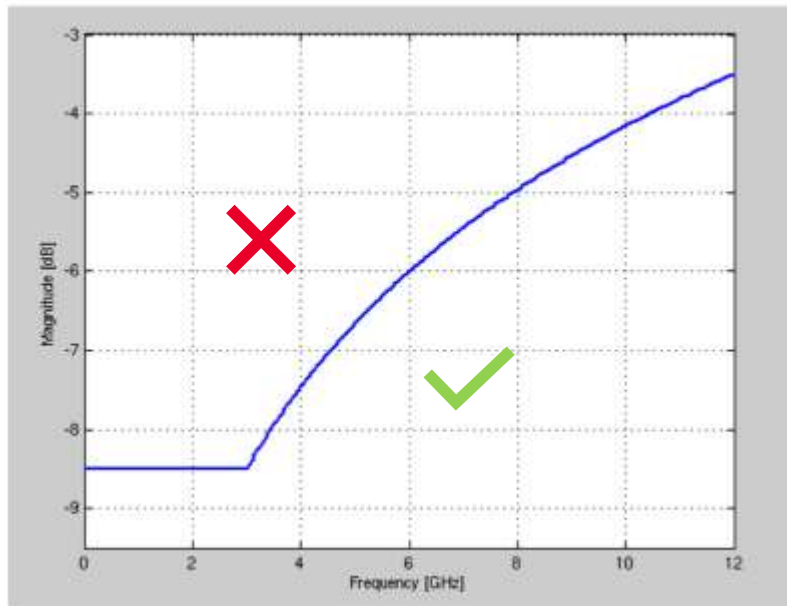


Return Loss

- TX and RX return loss
- Differential and Common Mode Return Loss
- **Challenge:** Very difficult to meet requirements, directly impacts TX and RX performance

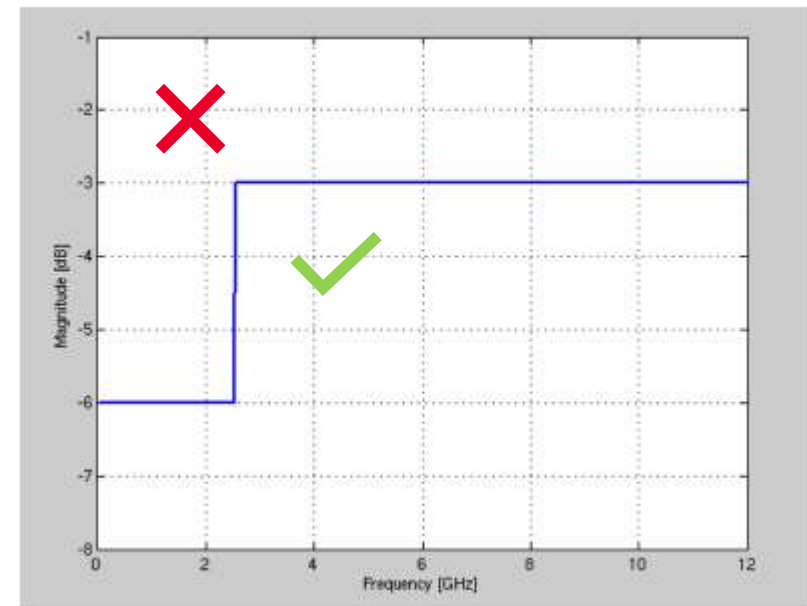
$$SDD22(f) = \begin{cases} -8.5 & 0.05 < f_{GHz} \leq 3 \\ -3.5 + 8.3 \cdot \log_{10}\left(\frac{f_{GHz}}{12}\right) & 3 < f_{GHz} \leq 12 \end{cases}$$

Figure 3-10. TX Differential Return Loss Mask



$$SCC22(f) = \begin{cases} -6 & 0.05 < f_{GHz} \leq 2.5 \\ -3 & 2.5 < f_{GHz} \leq 12 \end{cases}$$

Figure 3-11. TX Common-Mode Return Loss Mask

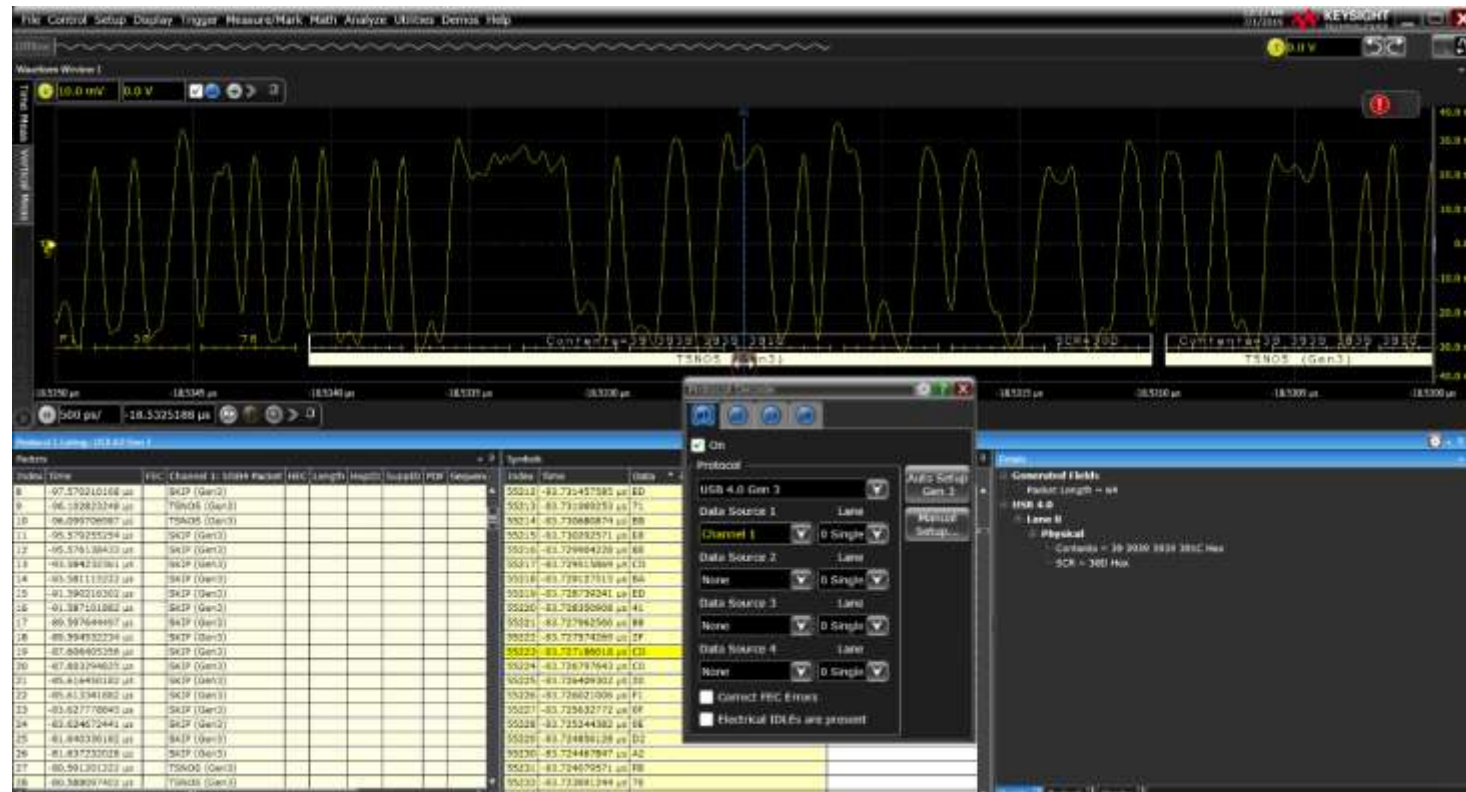


Current challenges between testing USB 3.2 x1 vs USB4

- Return Loss TX and RX
- Transmitter Equalization is not fixed and requires calibration
- Receiver Equalization is much more complex and requires optimization
- PHY bit rate doubles from 10 Gbps to 20 Gbps with significantly less margin
- Signaling on all 4 Type-C high-speed pairs
- Multiple bit rates: 10G, 20G and optionally 10.3125 and 20.625G
- Link management over the sideband channel
- Requirement for a passive, high-loss cable use case and short channel use case
- Retimer specific measurements
- New Jitter, Phase and Slew Rate Measurements
- Cross-talk Generation and Common Mode Interference
- Separate Jitter Cocktails for 10G/20G/TP2/TP3
- Built in Error Detector
- Link EQ Optimization prior to BER test
- Access to DUT status and error count over the sideband channel with Test Controller and USB4 Electrical Test Tool

Link Layer

- SBTX/SBRX in conjunction with high-speed TX/RX lanes are critical for link training
- **Challenge:** Incomplete view of Type-C signaling



USB4 Automated Electrical Transmitter Test

D9040USBC USB4 Tx Automated Test Software



Keysight UXR/V/Z Series Oscilloscope



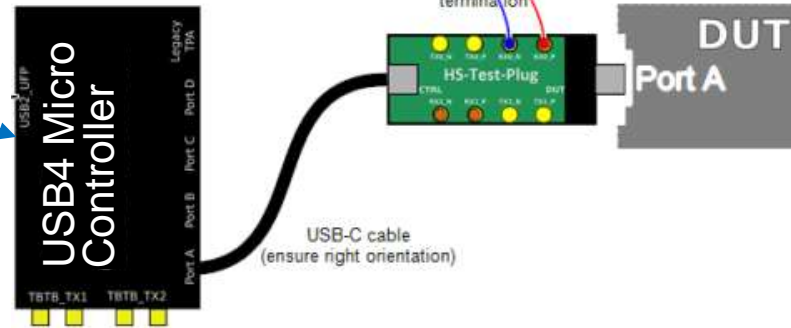
Example USB4 Test Pattern Changes
Rise/Fall Time: SQ128 (64 bit "1", 64 bit "0")



USB4ETT

```
Running the following test script may take a few minutes to complete. Please wait for the DUT response.
C:\USB4ETT\Microsoft Windows [Version 10.0.14393]
(c) 2015 Microsoft Corporation. All rights reserved.
C:\Program Files\Keysight\Infinium\Apps\USB4Test>cd C:\USB4ETT
C:\USB4ETT>USB4ElectricalTestTool.exe -T: TX -D: 1 -O: Receptacle -L0 -L1 -L: All -G3 -Pa SQ128 -Sw None
Elapsed Time: 00:00:01
```

Control data rate, Tx EQ preset and test pattern



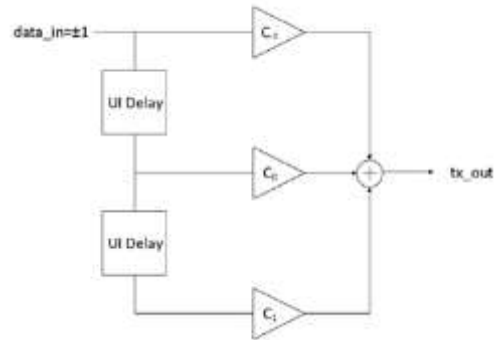
Measure both TP2, TP3+EQ Eye and Jitter
(Calculate TP3+EQ waveform in oscilloscope)

Eye Diagram Test: PRBS31



USB4 Automated Transmitter and Receiver Equalization Calibration

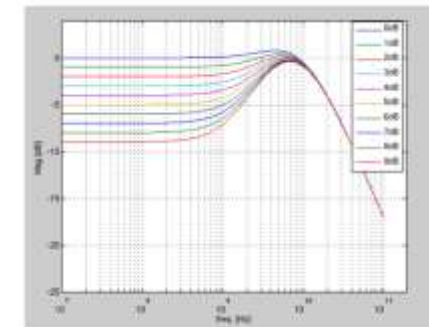
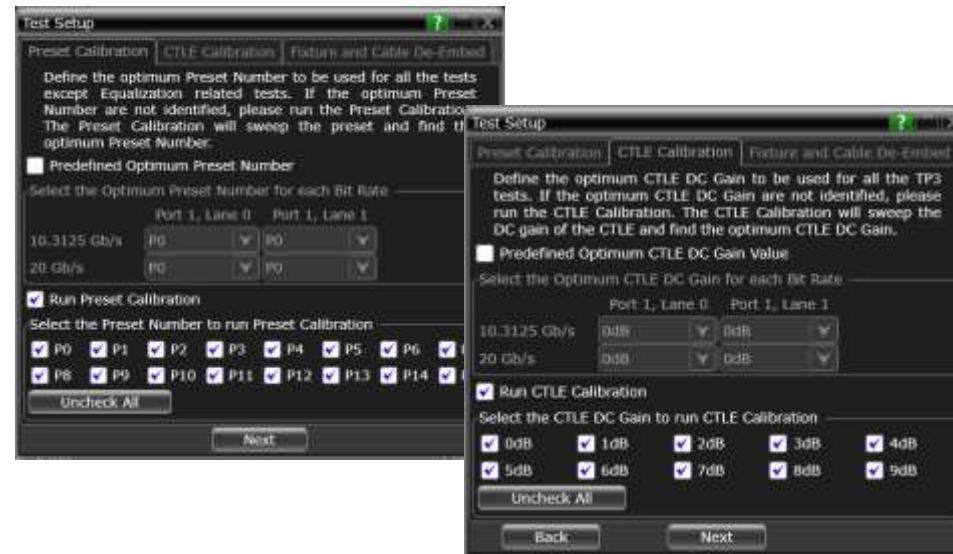
- Optimize TX FFE preset at TP3' → Select preset which minimizes DDJ (Data Dependent Jitter)
- Optimize RX CTLE DC gain + DFE at TP3 → Maximize the Eye Area (EW x EH)
- D9040USBC software automates these measurements and uses the optimal settings during tests



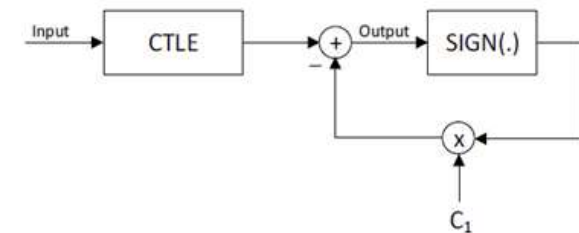
Transmitter Equalizer
3-tap FFE with 16 presets

Preset Number	Pre delay (UI)	Amplitude (dB)	Individual Tap Coefficients			
			C ₁	C ₂	C ₃	C ₄
0	0	0	0	0	0	0
1	0	-11.5	0	0	0.00	-0.19
2	0	-5.5	0	0	0.01	-0.17
3	0	-2.9	0	0	0.03	-0.22
4	0	-0.5	0	0	0.09	-0.25
5	0.0	0	-0.01	0.01	0	0
6	0.2	-12.8	-0.01	0.01	0.01	-0.04
7	0.4	-10.8	-0.01	0.01	0.02	-0.04
8	0.7	-10.8	-0.01	0.01	0.03	-0.02
9	1.0	-10.8	-0.01	0.01	0.04	-0.02
10	1.5	0	-0.01	0.01	0	0
11	2.0	-10.2	-0.01	0.01	0.01	-0.01
12	3.0	-10.2	-0.01	0.01	0.01	-0.01
13	4.0	-10.2	-0.01	0.01	0.01	-0.01
14	5.0	-10.2	-0.01	0.01	0.01	-0.01
15	6.0	-10.2	-0.01	0.01	0.01	-0.01

D9040USBC USB4 Transmitter Test software



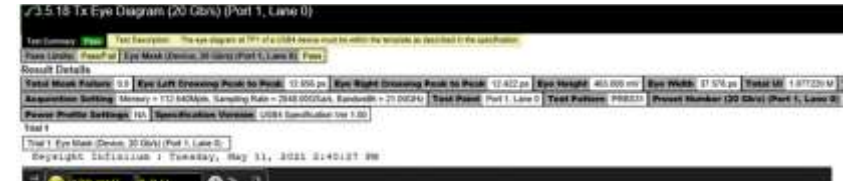
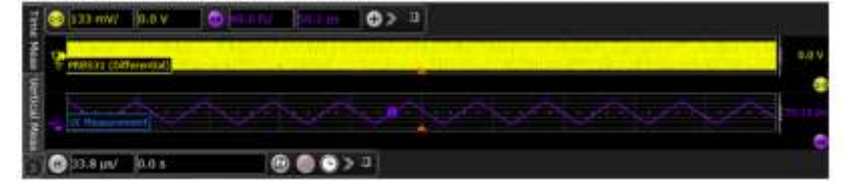
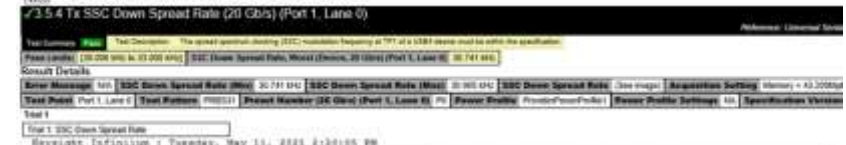
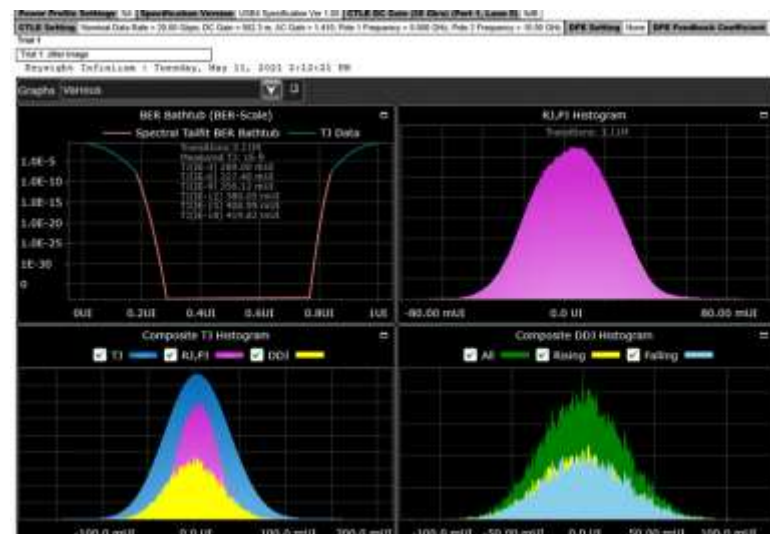
Receiver Equalizer
CTLE with 10 DC gain settings + DFE



D9040USBC Automated Test Suite and Test Reports

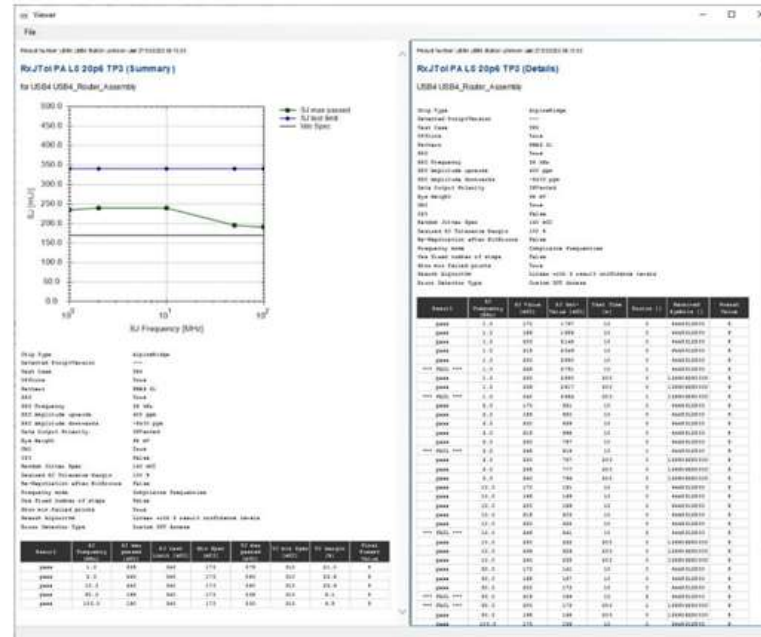
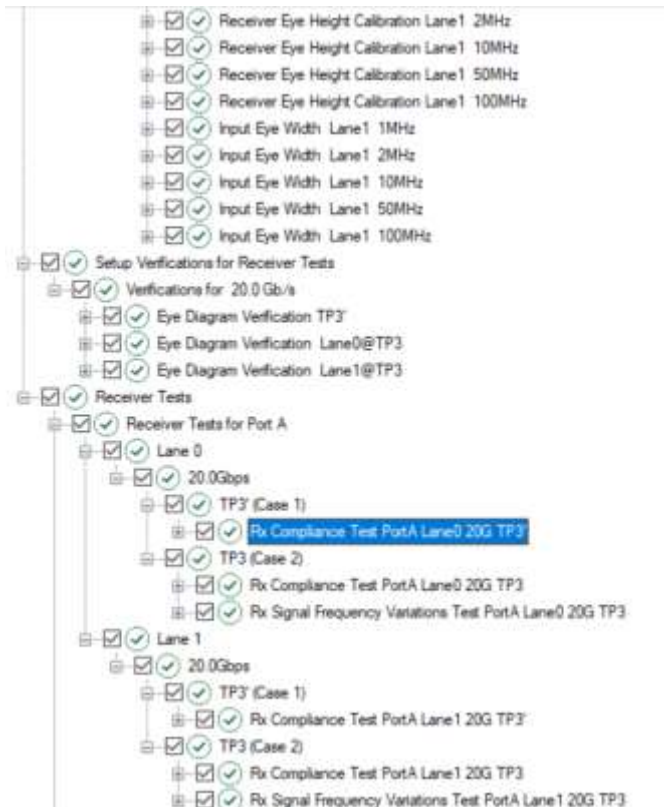
- USB 4 Transmitter Tests
 - Device Transmitter Tests (Port 1)
 - Device Transmitter Tests (10.3125 GB/s)
 - Tx Rise/Fall Time
 - Tx Rise Time (Lane 0)
 - Tx Fall Time (Lane 0)
 - Tx Rise Time (Lane 1)
 - Tx Fall Time (Lane 1)
 - Tx Jitter
 - Tx Uncorrelated Jitter, Uncorrelated Deterministic Jitter
 - Tx Total Jitter
 - Tx Unit Interval and SSC Modulation
 - Tx Unit Interval and SSC Down Spread Modulation
 - Tx SSC Phase
 - Tx AC Common Mode Voltage
 - Tx AC Common Mode Voltage (Lane 0)
 - Tx AC Common Mode Voltage (Lane 1)
 - Tx Eye Diagram
 - Tx Eye Diagram (Lane 0)
 - Tx Eye Diagram (Lane 1)
 - Tx Eye Diagram TP3 (Lane 0)
 - Tx Eye Diagram TP3 (Lane 1)
 - Tx Lane to Lane Skew
 - Tx Lane to Lane Skew (Lane 0/Lane 1)
 - Tx Equalization
 - Tx Equalization Preshoot (Lane 0)
 - Tx Equalization Preshoot (Lane 1)
 - Tx Equalization Deemphasis (Lane 0)
 - Tx Equalization Deemphasis (Lane 1)
 - Tx Swing Preset 15 (Lane 0)
 - Tx Swing Preset 15 (Lane 1)
 - Tx Electrical Idle Voltage
 - Tx Electrical Idle Voltage (Lane 0)
 - Tx Electrical Idle Voltage (Lane 1)

Pass #	Failed #	Test Name	Actual Value	Margin	Pass Limits
1	0	3.3.1a Tx Packet Collision (Port 1, Lane 0)	Pass		Pass/Fail
1	0	3.3.7a Tx CML Calibration (Port 1, Lane 0)	Pass		Pass/Fail
1	0	3.3.8a Tx Rise Time (Port 1, Lane 0)	22.545 ps	125.5 %	VALUE >= 10.000 ps
1	0	3.3.8b Tx Fall Time (Port 1, Lane 0)	22.905 ps	125.1 %	VALUE >= 10.000 ps
1	0	3.3.11 Tx Uncorrelated Jitter (Port 1, Lane 0)	167.5 mUI	46.0 %	VALUE <= 310.0 mUI
1	0	3.3.12 Tx Uncorrelated Deterministic Jitter (Port 1, Lane 0)	37.4 mUI	66.2 %	VALUE <= 110.0 mUI
1	0	3.3.14 Tx Duty Cycle Extension (Port 1, Lane 0)	2.9 mUI	90.3 %	VALUE <= 30.0 mUI
1	0	3.3.13 Tx Line Frequency Uncorrelated Deterministic Jitter (Port 1, Lane 0)	21.7 mUI	69.0 %	VALUE <= 10.0 mUI
1	0	3.3.17 Tx Uncorrelated Jitter TP3 (Port 1, Lane 0)	185.6 mUI	40.1 %	VALUE <= 310.0 mUI
1	0	3.3.18 Tx Uncorrelated Deterministic Jitter TP3 (Port 1, Lane 0)	38.2 mUI	76.0 %	VALUE <= 110.0 mUI
1	0	3.3.19 Tx Total Jitter (Port 1, Lane 0)	327.7 mUI	38.8 %	VALUE <= 460.0 mUI
1	0	3.3.16 Tx Total Jitter TP3 (Port 1, Lane 0)	458.0 mUI	23.6 %	VALUE <= 630.0 mUI
1	0	3.3.3a Tx Unit Interval Mean, Min (Port 1, Lane 0)	56.1242 ps	46.4 %	50.1102 ps <= VALUE <= 56.1404 ps
1	0	3.3.3b Tx Unit Interval Mean, Max (Port 1, Lane 0)	56.1242 ps	46.7 %	50.1102 ps <= VALUE <= 56.1404 ps
1	0	3.3.2a Tx Unit Interval, Min (Port 1, Lane 0)	56.0095 ps	3.8 %	50.0000 ps <= VALUE <= 50.2513 ps
1	0	3.3.2b Tx Unit Interval, Max (Port 1, Lane 0)	56.2394 ps	4.7 %	50.0000 ps <= VALUE <= 50.2513 ps
1	0	3.5.5 Tx SSC Down Spread Rate (Port 1, Lane 0)	30.100 mUI	76.3 %	30.000 mUI <= VALUE <= 30.000 mUI
1	0	3.5.4 Tx SSC (Down Spread Range) (Port 1, Lane 0)	457.3 mUI	42.5 %	400.0 mUI <= VALUE <= 500.0 mUI
1	0	3.5.8 Tx SSC Slow Rate (Port 1, Lane 0)	426.8 mUI	57.3 %	VALUE <= 1.0000 mUI
1	0	3.5.8 Tx SSC Phase Deviation (Port 1, Lane 0)	31.402 ns	8.2 %	2.000 ns <= VALUE <= 22.000 ns
1	0	3.5.14 Tx AC Common Mode Voltage (Port 1, Lane 0)	51.15 mV	48.0 %	VALUE <= 100.00 mV
1	0	3.5.15 Tx Eye Diagram (Port 1, Lane 0)	Pass	100.0 %	Pass/Fail
1	0	3.5.19 Tx Eye Diagram TP3 (Port 1, Lane 0)	Pass	100.0 %	Pass/Fail
1	0	3.5.1a Tx Equalization Preshoot (Port 1, Lane 0)	Pass	100.0 %	Pass/Fail
1	0	3.5.1b Tx Equalization Deemphasis (Port 1, Lane 0)	Pass	100.0 %	Pass/Fail
1	0	3.5.1c Tx Swing Preset 15 (Port 1, Lane 0)	5.3750 dB	42.7 %	2.0000 dB <= VALUE <= 4.0000 dB



USB4 Automated Electrical Receiver Test

- Support both M8020A and M8040A High Performance J-BERT
- **N5991U40A** USB4 Receiver Test Software
- USB-IF USB4 Electrical Test Tool fully integrated



M8020A J-BERT + M8062A 32G front-end



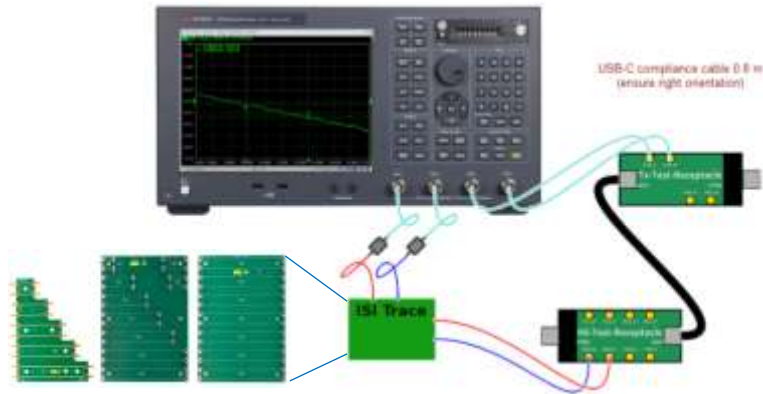
M8040A 32/64 Gbaud J-BERT

USB4 Automated Stress Signal Calibration

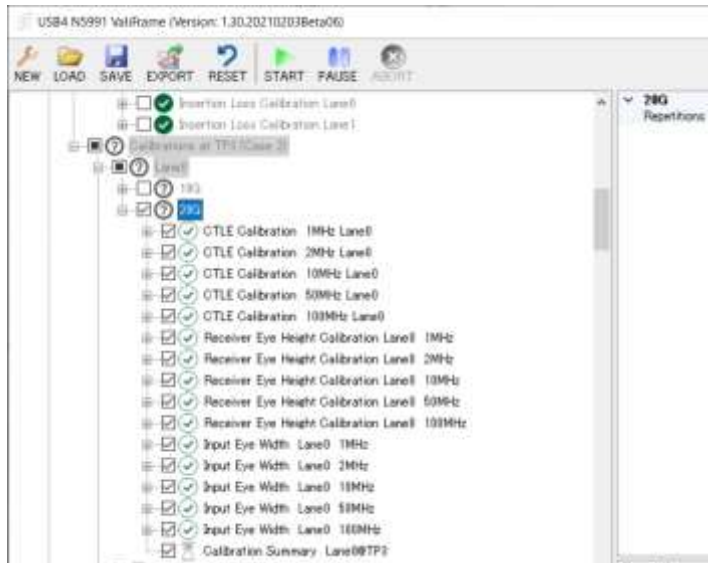
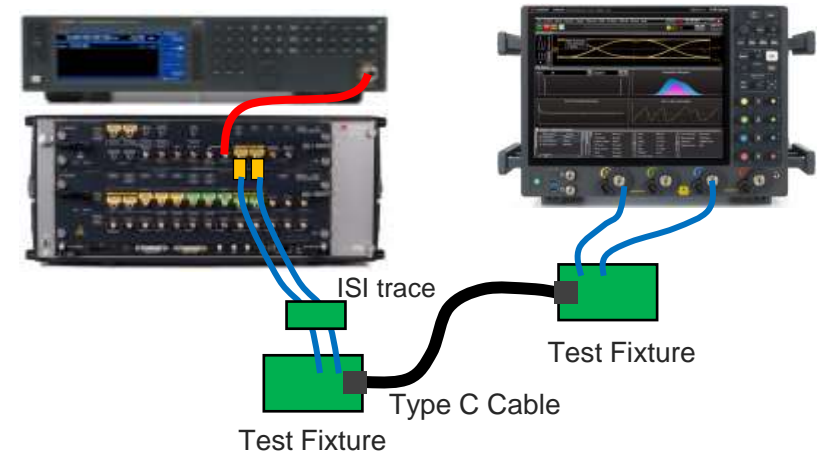
1 Case 1: Short Channel



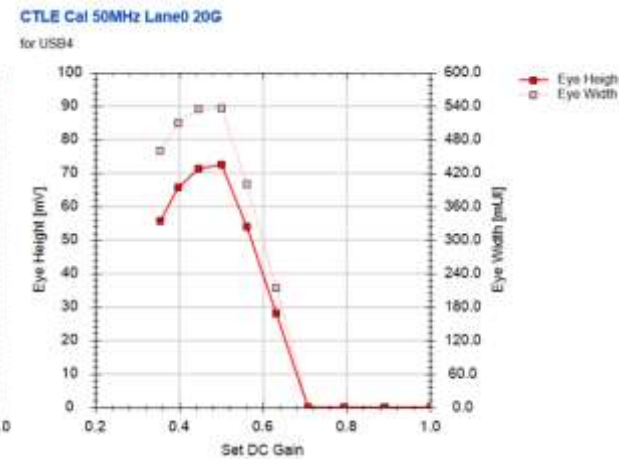
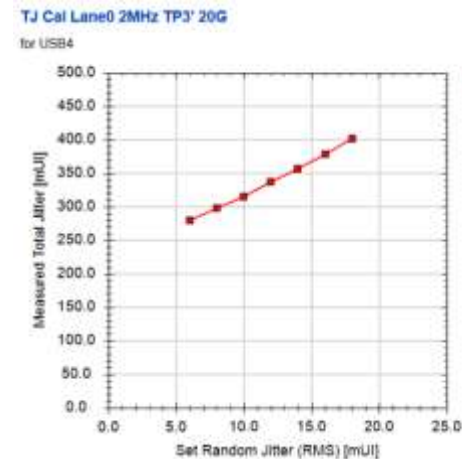
2 Long Channel Insertion Loss



3 Case 2: Long Channel

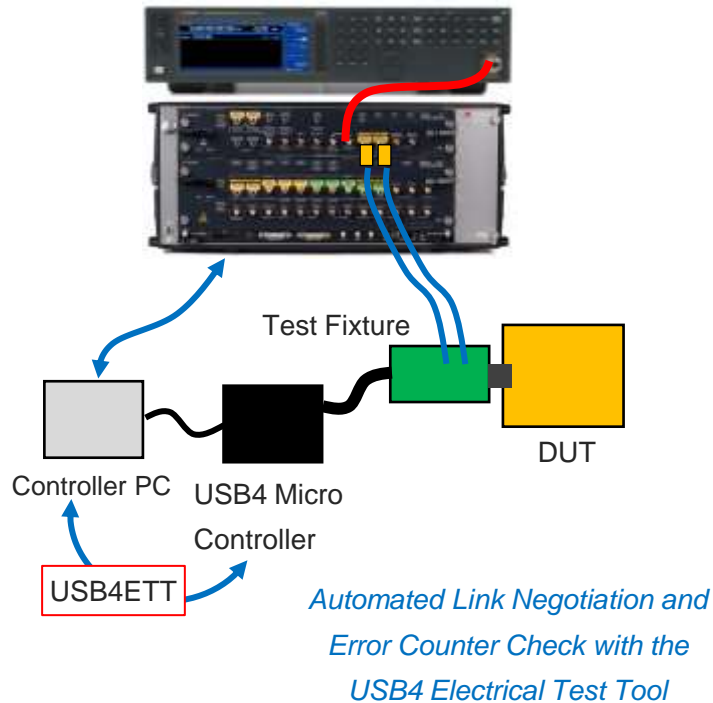


N5991U40A
USB4 Receiver
Test Software

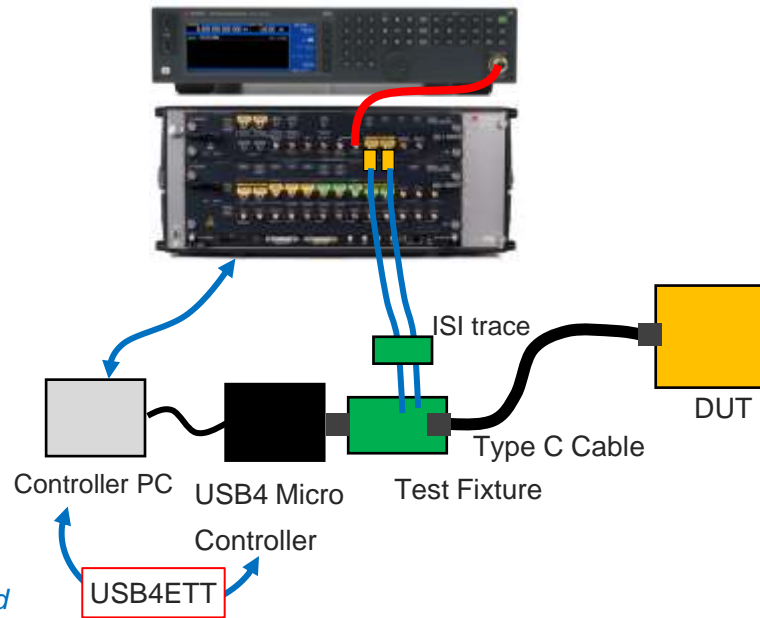


USB4 Automated Receiver BER Test

Case 1: Short Channel



Case 2: Long Channel

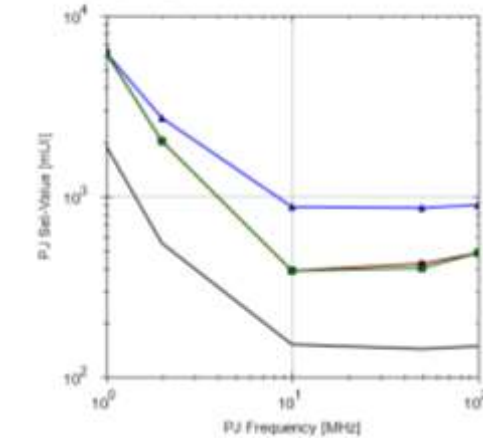


Communication DUT ↔ USB4ETT

Time	Event	Value
00:00:00	Starting BER test for 1	0
00:00:01	Starting BER test for 10	0
00:00:02	Starting BER test for 100	0
00:00:03	Starting BER test for 1000	0
00:00:04	Starting BER test for 10000	0
00:00:05	Starting BER test for 100000	0
00:00:06	Starting BER test for 1000000	0
00:00:07	Starting BER test for 10000000	0
00:00:08	Starting BER test for 100000000	0
00:00:09	Starting BER test for 1000000000	0
00:00:10	Starting BER test for 10000000000	0
00:00:11	Starting BER test for 100000000000	0
00:00:12	Starting BER test for 1000000000000	0
00:00:13	Starting BER test for 10000000000000	0
00:00:14	Starting BER test for 100000000000000	0
00:00:15	Starting BER test for 1000000000000000	0
00:00:16	Starting BER test for 10000000000000000	0
00:00:17	Starting BER test for 100000000000000000	0
00:00:18	Starting BER test for 1000000000000000000	0
00:00:19	Starting BER test for 10000000000000000000	0
00:00:20	Starting BER test for 100000000000000000000	0
00:00:21	Starting BER test for 1000000000000000000000	0
00:00:22	Starting BER test for 10000000000000000000000	0
00:00:23	Starting BER test for 100000000000000000000000	0
00:00:24	Starting BER test for 1000000000000000000000000	0
00:00:25	Starting BER test for 10000000000000000000000000	0
00:00:26	Starting BER test for 100000000000000000000000000	0
00:00:27	Starting BER test for 1000000000000000000000000000	0
00:00:28	Starting BER test for 10000000000000000000000000000	0
00:00:29	Starting BER test for 100000000000000000000000000000	0
00:00:30	Starting BER test for 1000000000000000000000000000000	0

RxJToI PA L0 20G TP3 (Summary)

for USB4_USB4_Router_Assembly



Automated JTOL margin test

N5991U40A
USB4 Receiver Test Software

Detailed test report

Result	PJ Frequency [MHz]	AC CM Set Amplitude [mV]	PRBS Set Amplitude [mV]	RJ Set Value (RMS) [mUI]	PJ Set Value [mUI]	Final Preset Value	Error counter check 1st Run	passed negotiations	Component	Errors 1st Run	Symbol count 1st Run	Error counter check 2nd Run	Errors 2nd Run	Symbol count 2nd Run
pass	1	1001	1094	15.60	1907	0	Pass (3 of 3)	4	Router	0	124808413194	-	-	-
pass	2	1001	1067	16.10	551	12	Pass (3 of 3)	4	Router	0	124799686618	-	-	-
pass	10	1001	1158	16.30	152	12	Pass (3 of 3)	4	Router	0	124816857602	-	-	-
pass	50	1001	1160	16.30	144	0	Pass (3 of 3)	4	Router	0	124793236729	-	-	-
pass	100	1001	1165	10.60	196	12	Pass (3 of 3)	4	Router	0	124800063933	-	-	-

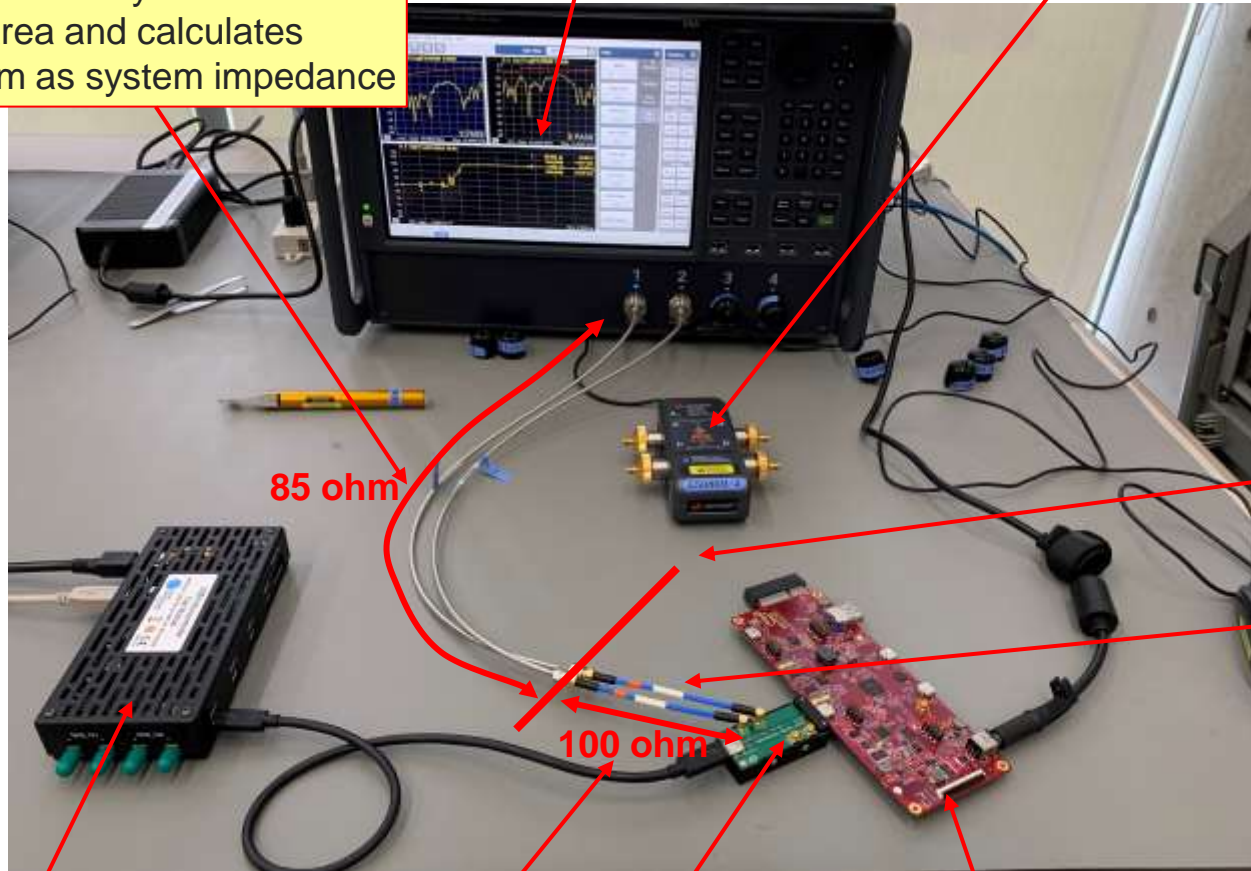
USB4 Return Loss Test

Test Setup Example

Network Analyzer calibrates this area and calculates 85ohm as system impedance

E5080B Network Analyzer

N4433D E-cal



85 ohm

100 ohm

Test Controller

Test Fixture

USB4 DUT

Remains extra reflection as 100ohm differential impedance

Calibration Plane

USB4 Tx Differential Impedance Example



SMP-2.92mm Cable

USB4 DUT

DUT's Source Termination

Test Fixture

Type C connector

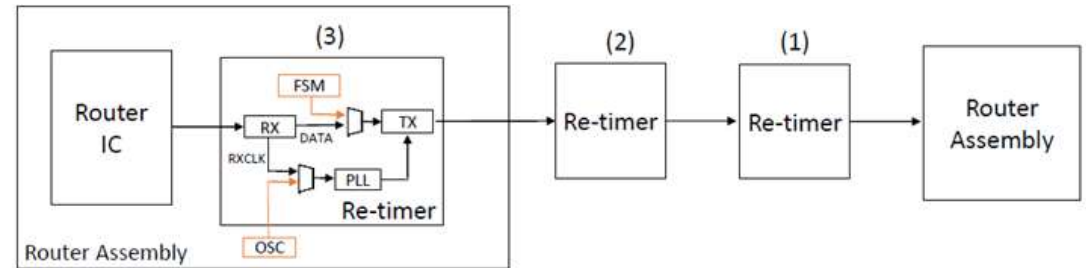
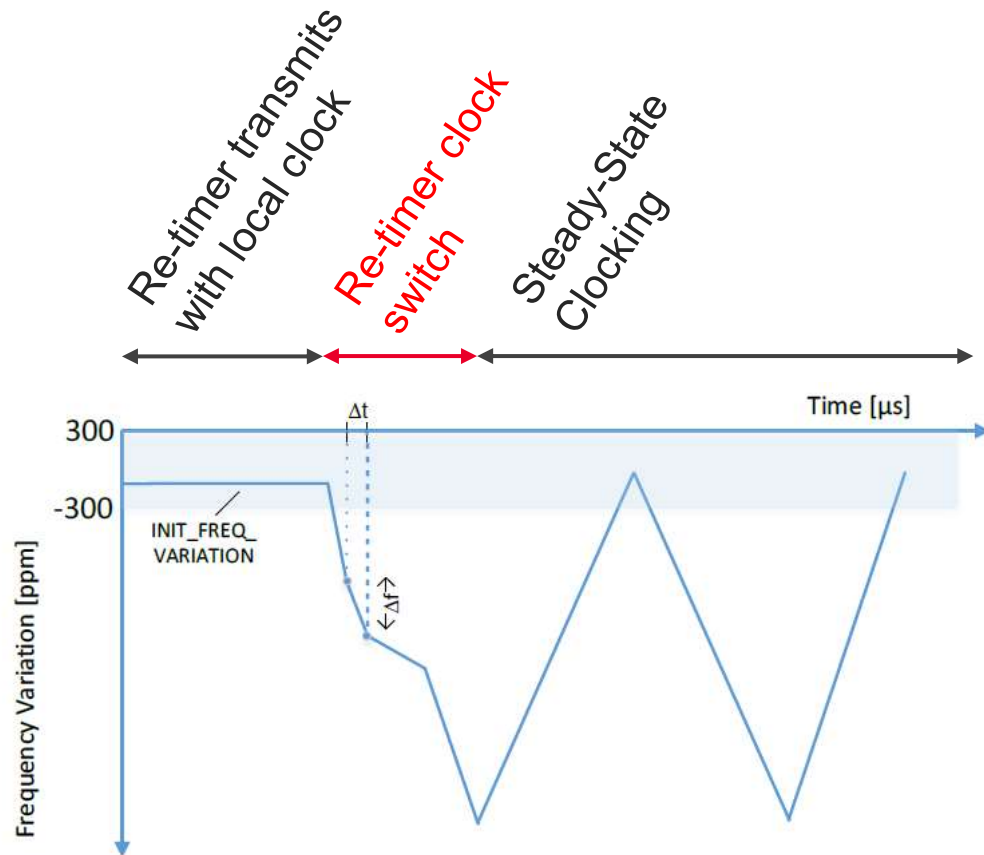
Calibration Plane

SMP-2.92mm Cable

Need to compensate this extra 100ohm area by "Gating" option of network analyzer

USB4 Signal Frequency Variation Test

USB4 Spec defines the Signal Frequency Variation Limit in Link Training for the System including Re-timers

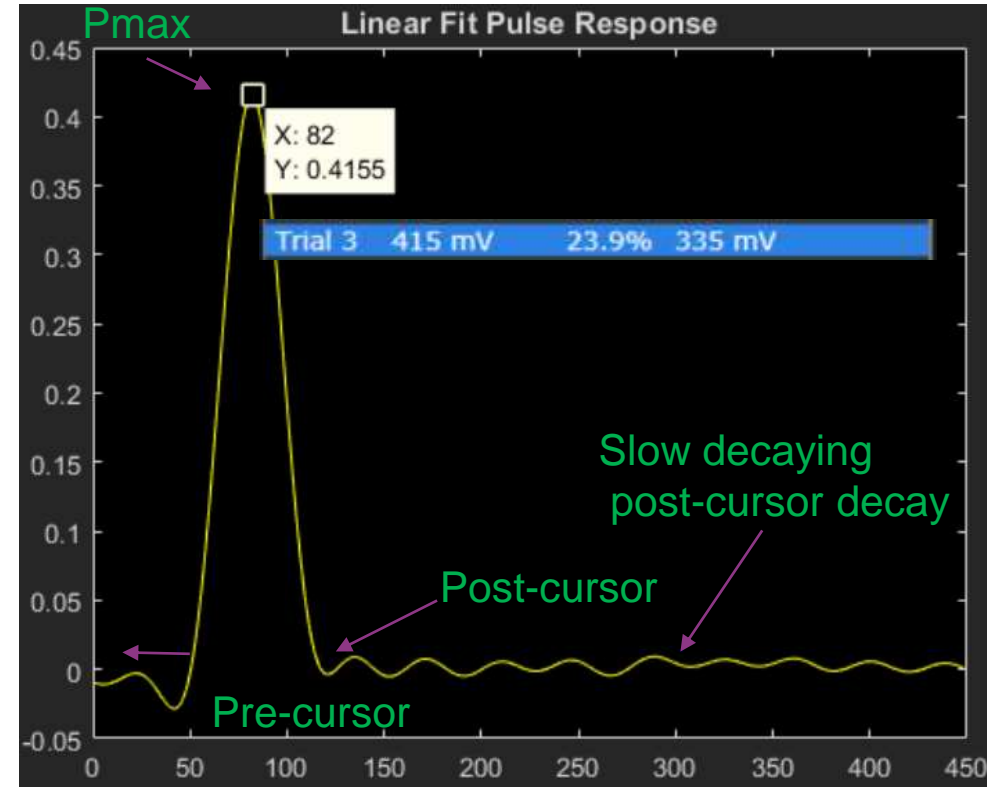


Signal Frequency Variation Test

- Tx** Verify that a transmitter's frequency variation during link training falls within the limit.
- Rx** Verify that a receiver does not lose CDR lock when the frequency variation takes place.

What happens after USB4 – PAM4?

- SNDR (Signal Noise Distortion Ratio)
 - LFPR (Linear Fit Pulse Response)
 - Sigma e
 - Sigma n
- R_{LM} (Level Separation Mismatch Ratio)
- TX ISI (Transmitter Output Residual ISI)
- PRBS13Q Patterns



✓ Signal-to-noise-and-distortion ratio

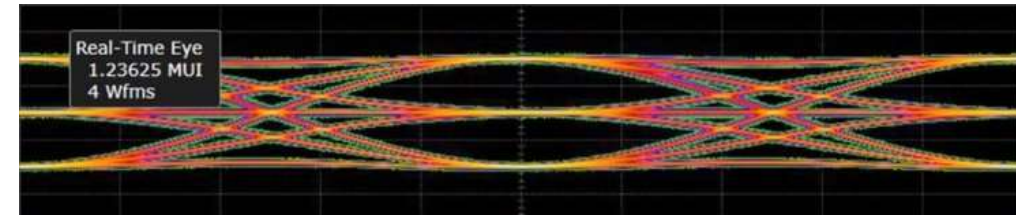
Test Summary: **Pass** Test Description: Measures the SNDR

Pass Limits: **>= 31.000 dB** Signal-to-noise-and-distortion ratio - IEEE802.3bs TP0a **36.139 dB**

Result Details

Pmax	427.870 m	Sigma e	5.517 m	Sigma n	3.755 m
------	-----------	---------	---------	---------	---------

$$SNDR = 10 \log_{10} \left(\frac{P_{\max}^2}{\sigma_e^2 + \sigma_n^2} \right)$$



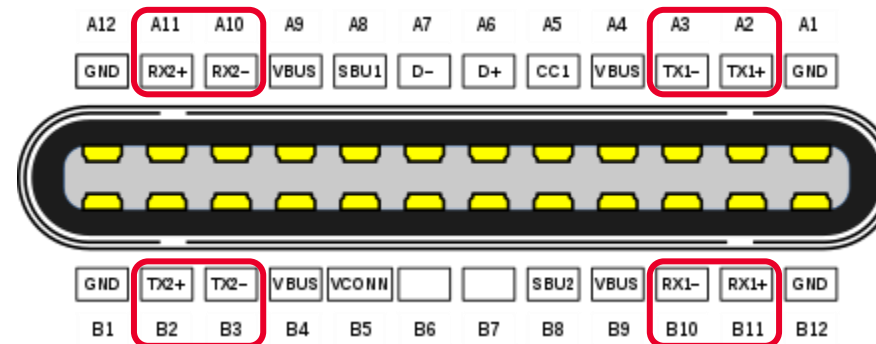
The Industry's Best Signal Integrity

- **10 bits ADC, 256 GSa/s**
- **Lowest noise**
 - < 900 μV rms @ 110 GHz
 - < 500 μV rms @ 70 GHz
 - < 300 μV rms @ 33 GHz
- **Lowest intrinsic jitter**
 - 20 fs rms
- **Lowest inter-channel jitter**
 - 10 fs rms
- **Highest ENOB**
 - > 5.0 bits @ 110 GHz
 - > 5.4 bits @ 70 GHz
 - > 5.9 bits @ 33 GHz



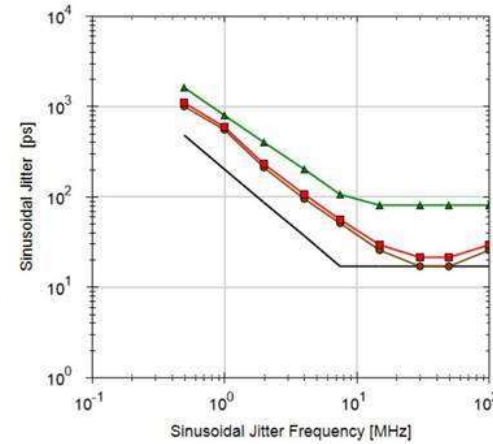
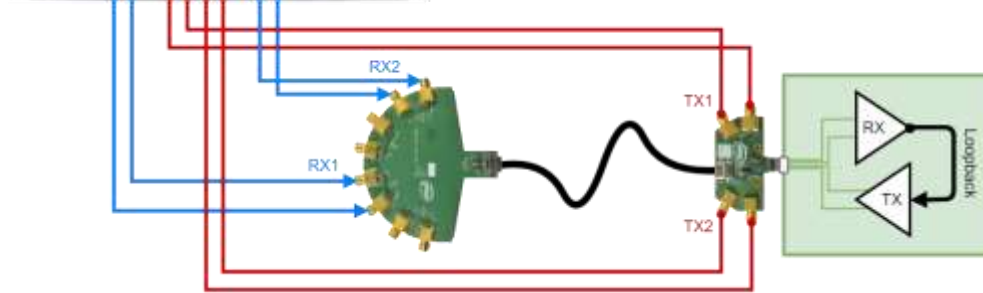
USB 3.2 Specification Update

- **New** dual lane (x2) mode over USB-C®
 - 5 Gb/s x2 → 10 Gb/s
 - 10 Gb/s x2 → 20 Gb/s
- The x2 capability is negotiated during the LBPM handshake
- All four high-speed lanes of the interface active
 - Additional crosstalk
 - Performance degradation

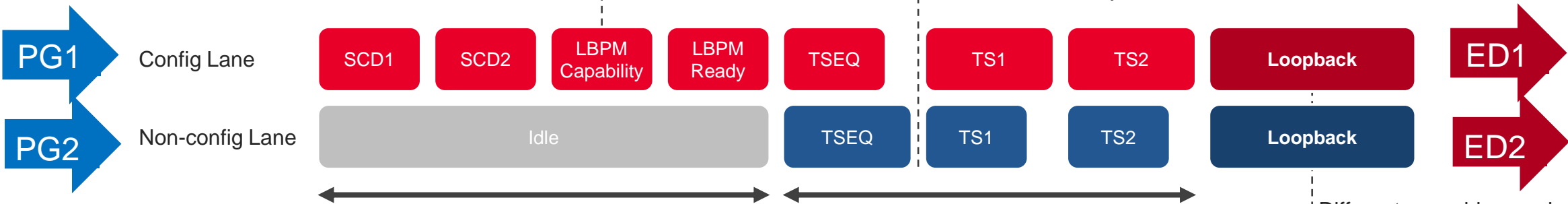
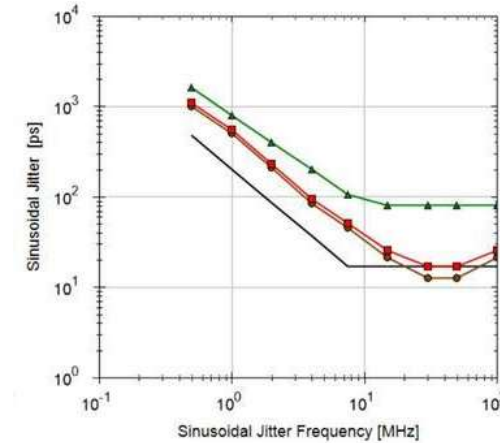


Best Known Method of x2 Receiver Testing

- Two Pattern Generators / Error Detectors
- Two independent RX paths fully calibrated
- Link Training in x2 mode
- Concurrent JTOL on both RX lanes
- USB-like traffic during test
- Test setup closest to operating condition



x1 vs x2



Different scrambler seed per lane to maximize crosstalk

Type-C Active Link Access, Automated Protocol Trigger Decode

Provides access to all Type-C signals during an active link.

Signals include Vbus, USB 2.0, USB-PD, SBU1/2, and TX/RX up to maximum USB4 rate of 20 Gbps.

Works in conjunction with D9010USBP Keysight Protocol Trigger Decode solutions for USB-PD, eUSB2, USB 2.0, USB 3.2, USB4 and DP AUX.



N7019A Usage

Measure Low Speed Signal (SBTX/SBRX) and Decode



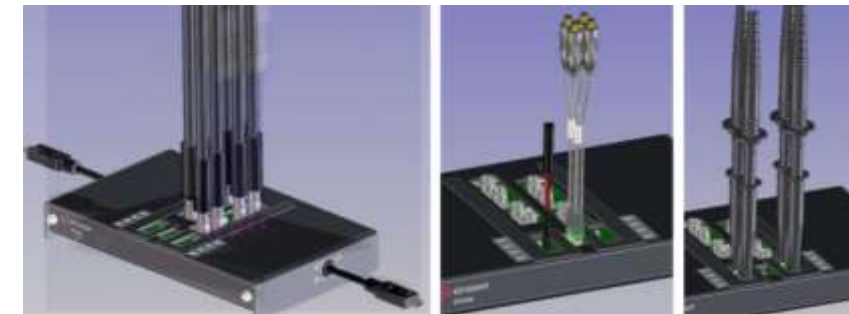
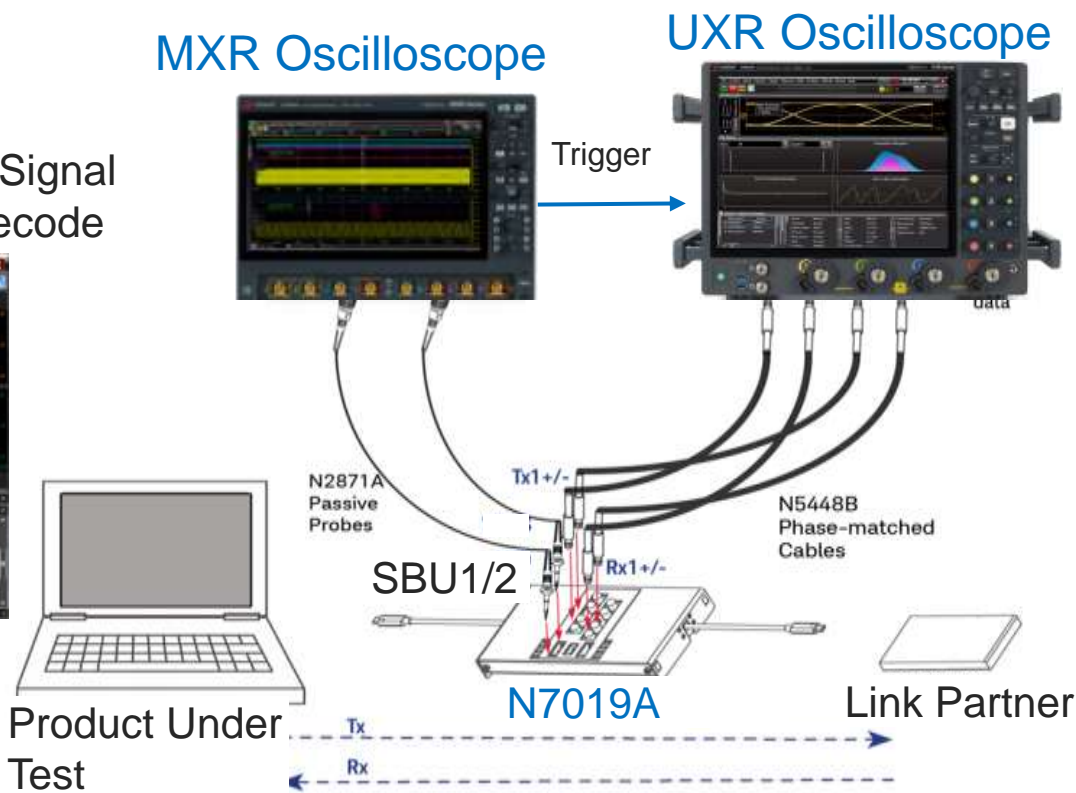
MXR Oscilloscope



UXR Oscilloscope



Measure High Speed Signal (TX1/RX1, TX2/RX2) and Decode



USB4 Related Solutions: DisplayPort UHBR

D9042DPPC

DisplayPort UHBR
Source Test Software



TX/RX EQ optimization, link training and test procedures

DUT

AUX CH
Controller

N5991DP2A

DisplayPort
Sink Test Software



Stress signal calibration, link training and BER test

DUT

AUX CH
Controller



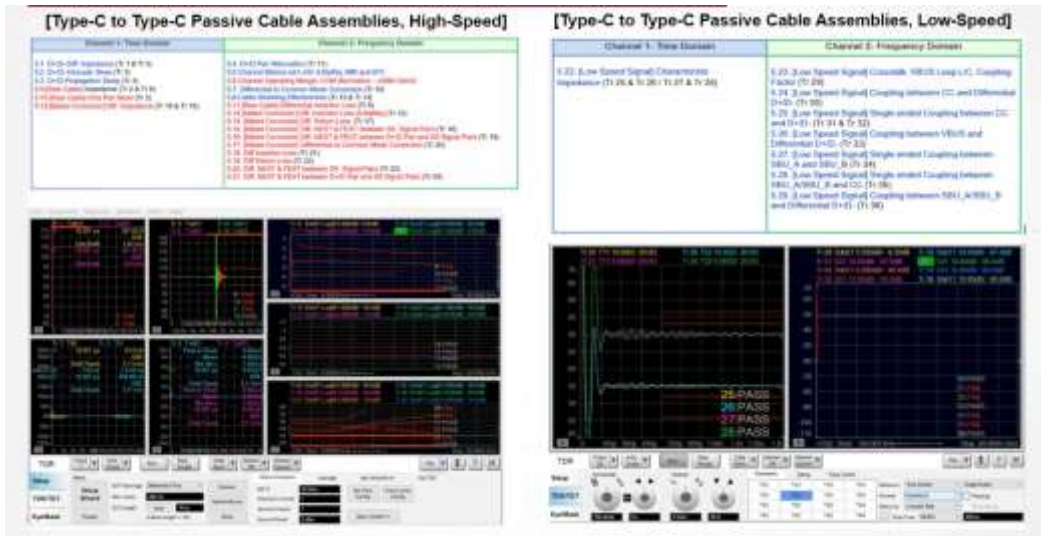
UXR Series
Oscilloscope



M8000 Series
J-BERT

USB4 Related Solutions (cont.)

- USB 3.2 x2 (dual lane)
- Passive Cables for USB 3.2, USB4, DisplayPort
- LRD: Discrete, Embedded and Cable for USB 3.2, USB4, DP
- Retimer: Discrete, Embedded and Cable for USB 3.2, USB4, DP
- RFI



Technology Standards		Available MCF & State Files	
		Connectors and Cable Assemblies	Tx/Rx Hot TDR
USB	USB2.0	E5071C E5080B	N/A
	USB3.0	E5071C E5080B	N/A
	USB3.1	E5071C E5080B	N/A
	USB4.0 / USB Type-C	E5071C M837xA E5080B	E5071C E5080B
HDMI	HDMI 1.4b	E5071C	E5071C
	HDMI 2.0	E5071C	E5071C
	HDMI 2.1	E5071C M837xA	E5080B
SATA	v3.0	E5071C	E5071C
DisplayPort	v1.2b	E5071C	N/A
	v1.3	E5071C	N/A
Thunderbolt	Thunderbolt 3	N/A	E5071C

USB Type-C radio frequency interference (RFI) test

Why do we test RFI at USB Type-C ports?

USB 2.0 signaling may cause radio frequency interference, that degrades the performance of wireless systems in the same assembly.

- Reducing the signal-to-noise ratio at the radio receiver
- Negatively impact the response of wireless module, WiFi, or 4G/LTE data throughput and range

Method-of-Implementation (MOI) with Keysight N9000B CXA signal analyzer

Keysight N9000B Signal Analyzer

Shunt Box

DUT

RFI System Test Fixture

HSD Cable Test Challenges

CURRENT MARKET SITUATION



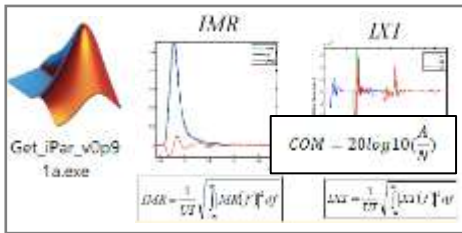
Multiport

- Increase of device complexity that demand for multiport.
 - USB4/USB Type-C & DisplayPort required 20-ports
- True multi-port system is too expensive: >\$300K for 20-ports PXI-VNA.
- No software automation for multiport, calibration and test execution are still manual.



Long Setup Time

- Calibration is complicated for custom switch solution.
- Compliance test procedures are tedious and prone to operation error.
EG: USB4/USB Type-C passive cable required 44-sets of s4p for HS test manually, one cable sample could take 3-5 hours to complete.



Compliance Test Tool

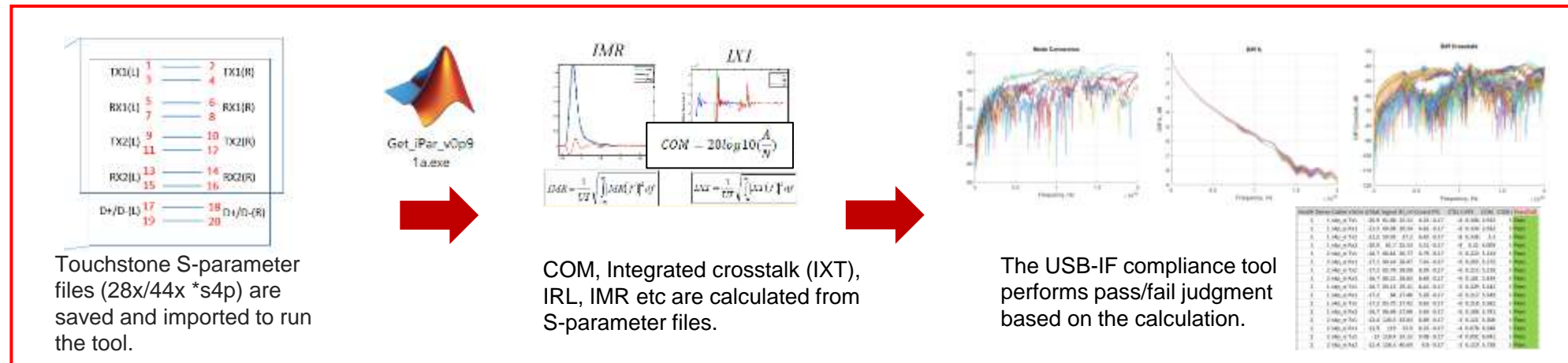
- USB-IF and VESA required compliance test tools to verify the integrated S-Parameters and COM results (Get_iPar and IntePar Matlab tools).
- Manual file configuration and setup to run the tools to determine final compliance results.

USB4/USB 3.2 Active/Passive Cable Compliance

New COM test requirement for USB4-Gen3

Test Parameters	Passive Cable	Active Cable	Active Component
Channel Operating Margin (COM)	Normative	Normative	Not required
ILfitatNq	Normative	Normative	Not required
Integrated Multi-Reflection (IMR)	Informative	Normative	Not required
Integrated Return Loss (IRL)	Normative	Normative	Informative
Integrated Crosstalk (IXT for INEXT & IFEXT)	Normative	Not required	Informative
Integrated Crosstalk (IXT for IDXT)	Normative	Not required	Not required

Manual steps to run Get_iPar tool = Time consuming (3-5 hours) and prone human error!



* Same steps applied for USB Type-C Passive cable compliance test – Channel Metrics/COM.

Keysight Automated Test Solution

KEY FEATURES

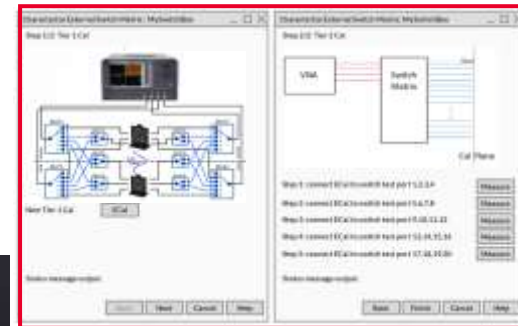
- Affordable price compared to true multiport PXI-VNA system.
- Fully automated switch matrix control without any cable/port reconnection.
- Auto calibration and de-embedding wizards.
- PathWave TAP based compliance software for automation and test sequencing.
- Comprehensive HTML reports with result table and waveform diagrams.
- Supports Keysight E5080B, Streamline USB/TBT Series VNA and PXI-VNA.
- Compliance test by HSD module:
 - USB Type-C (First Release)
 - DisplayPort
 - HDMI

Hardware solution are available for order NOW!

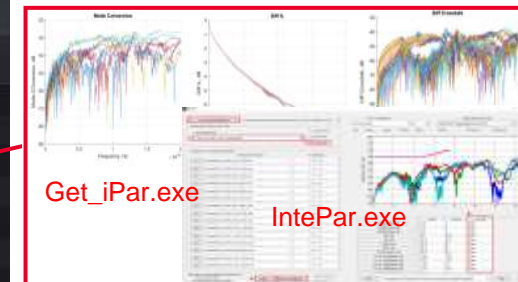


Keysight Automated Cable Test

KEY FEATURES PREVIEW



Guided connection and setup diagram



Auto-compliance tool in single platform



Real-time trouble-shooting



HTML/CSV test report

KEYSIGHT Test Automation

File Settings Tools View Help

Compliance Test Setup

- Select Standard: USB Type-C
- Select Cable and Connector: Type-C to Type-C Cable Assemblies
- Select USB Generation: USB4 Gen3

Test Fixture: Fixture Setup... Characterize

System: System Setup... Calibration

Optimize Number of Connections

Test Plan: USB_Type-C_to_Type-C_Passive_Cable_Assembly_USB4-Gen3*

Completed in 256 s

Name	Verdict	Informative	Tool	Duration	Flow
High-Speed (High-Speed Test Fixture)	Pass			151 s	
Channel Metrics (ILflatNq)	Pass		Get_iPar	151 s	
Channel Metrics (IRL)	Pass		Get_iPar	1.41 ms	
Channel Metrics (C2D, D2C)	Pass		Get_iPar	1.35 ms	
Channel Metrics (IMR)	Informative		Get_iPar		
Channel Operating Margin (COM)	Pass		Get_iPar	4.02 ms	
Channel Metrics (IXT: INEXT, IFEXT)	Pass		Get_iPar	1.39 ms	
Channel Metrics (IXTL_DP, IXTL_USB)	Pass		Get_iPar	4.18 ms	
Channel Metrics (IDDXT_1NEXT + FEXT, IDDXT_2NEXT)	Pass		Get_iPar	1.39 ms	
Differential Insertion Loss	Informative				
Differential Return Loss	Informative				
Differential Near-End and Far-End Crosstalk between TX/RX Pair	Informative				
Differential Crosstalk between D+/D- and TX/RX Pairs	Informative				
USB D+/D- (High-Speed Test Fixture)	Pass			564 us	
D+/D- Differential Impedance	Pass			151 us	
D+/D- Intra-Pair Skew	Pass			54.6 us	
D+/D- Propagation Delay	Pass			84.4 us	
D+/D- Pair Attenuation	Pass			74.4 us	
Low-Speed (Low-Speed Test Fixture)	Pass			102 s	
Cable Shielding Effectiveness (EMI/RFI Test Fixture)	Pass			2.67 s	

Log

Errors 0 Warnings 0 Information 883 Debug 66

```

18:03:13.309 TestPlan
18:03:13.311 TestPlan Starting TestPlan 'USB_Type-C_to_Type-C_Passive_Cable_Assembly_USB4-Gen3' on 10/25/2021 18:03:13, 31 of 64
18:03:13.326 KtVNACT VNA Simulator Connected
18:03:13.326 KtVNACT Resource "KtVNACT (TCP/IP@:localhost::hislip@:INSTR)" opened. [13.3 ms]
18:03:13.326 KtVNACT Resource "KtVNACT" opened. [13.3 ms]
    
```

Select DUT Type
System Setup & Guided
Calibration
Test Fixture Setup &
Characterize (measure s2p)

Setup in Single Panel!

First fully automated compliance test solution in the market!

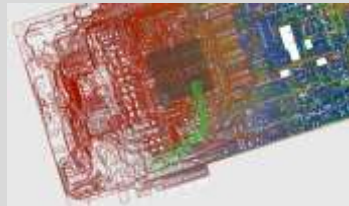
Keysight Type-C Solutions Matrix

Design Simulation, Protocol Decode, Live Link Debug, USB-PD, RF, Channel Characterization, SBU, USB, Thunderbolt, DisplayPort

Physical Layer System Simulation



ADS Design Software



SIPro/PIPro



Simulation to measurement correlation

Transmitter Test Active Cable Test

Automated Standards Test Software



UXR Infiniium Scope
<1mV RMS
<25fs RMS



TX Test Fixture

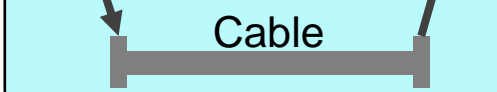


Interconnect Test Return Loss Test

E5080B ENA with S96011A Enhanced TDR software



Active/Passive Cable



Receiver Test Active Cable Test

Automated Standards Test Software



M8000 J-BERT
<200fs RMS

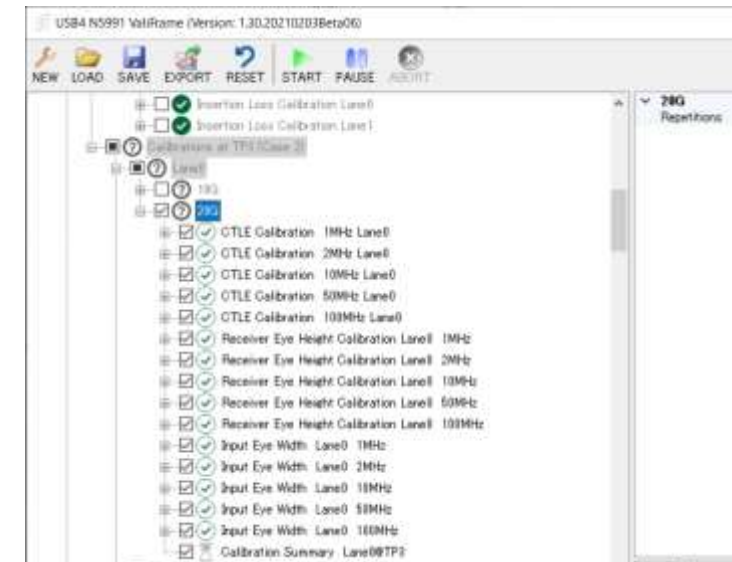


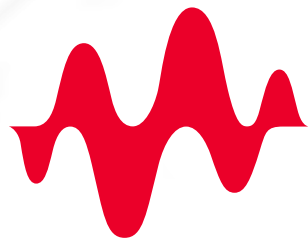
RX Test fixture



Best Solution for USB4 and Beyond

- UXR: best signal integrity, lowest noise, same argument as PCIe
 - Supports next-generation technologies with multi-level signaling
 - Most accurate jitter and noise analysis tools
 - Advanced equalization and math functions
- RX test solution supports M8020A and M8040A
 - Lowest intrinsic RJ in the market
 - Multi-tap FFE for accurate equalization
 - The M8040A supports next-generation technologies with multi-level signaling
- Keysight has been used to certify the vast majority of shipped TBT3/USB4 products
- TX and RX test automation software
 - SigTest and USB4 Electrical Test Tool (USB4ETT) fully integrated
 - Easy configuration and operation
 - Unattended test execution
- Unique product N7019A with D9010USBP protocol decode software
 - Examine all 24 pins of the USB Type-C interface: high-speed lanes, SBU, CC, power, etc.
 - Debug link bring-up issues on a live link between two products
 - Covers the entire USB Type-C ecosystem: USB PD, USB 2.0, USB 3.2, USB4, DP1.4a, DP2.1 (coming)





KEYSIGHT
TECHNOLOGIES

4.50221